Chapter 4

Analysis and design of power subsystem

Abstract

In this chapter, a more detailed analysis of the system is made. All the circuitries are analyzed and computations are made. It is performed a analysis of the housekeeping data and the signals acquired for this. The hardware and the software used for Microcontroller Unit (MCU) are detailed.

4.1. Introduction

In this chapter, the design of the PSU is documented and detailed analysis is completed. In section 3.2, it was chosen the topology for PSU, as shown. In this respect, in the following, each part is detailed and physical implementation solution is presented.

The chapter is triturated after the most significant parts which consists the PSU. The circuits are presented as well as the devices. Then, for each part, if they require some specific computations, the formulas and results are presented. Finally, a conclusion is stated.

4.2. MPPT converter and battery charger

As described in Chapter 3, Section 3.4.1, the maximum power point tracker is an electronic device which optimizes the point of operation of the solar cells in order to achieve maximum power delivered by the solar cells.

The implementation solution implies a converter, to step-up the voltage from the solar cells, and which will provide the voltage to the unregulated bus. This converter is controlled by the positive feedback of the output current. Maximum power point tracking for such a PV system, with battery back-up is achieved by employing this simplified positive feedback control strategy to maximize the output current into the battery.

For all the devices, datasheet can be found on the attached CD of the project.

The step-up switching controller (MAX1771) provides 90% efficiency over a 30mA to 2A load. A unique current-limited pulse-frequency-modulation (PFM) control scheme gives this device the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using less than 110µA of supply current (vs. 2÷10mA for PWM converters). This controller uses miniature external components. Its high switching frequency (up to 300kHz) allows surface-mount magnetics of 5 mm height and 9 mm diameter. It accepts input voltages from 2V to 16.5V. The output voltage is preset at 12V, or can be adjusted using two resistors. The MAX1771 optimizes efficiency at low input voltages and reduces noise by using a single 100mV current-limit threshold under all load conditions. The MAX1771 drives an external N-channel MOSFET switch, allowing it to power loads up to 24W. A functional diagram for the device can be seen in the figure below.

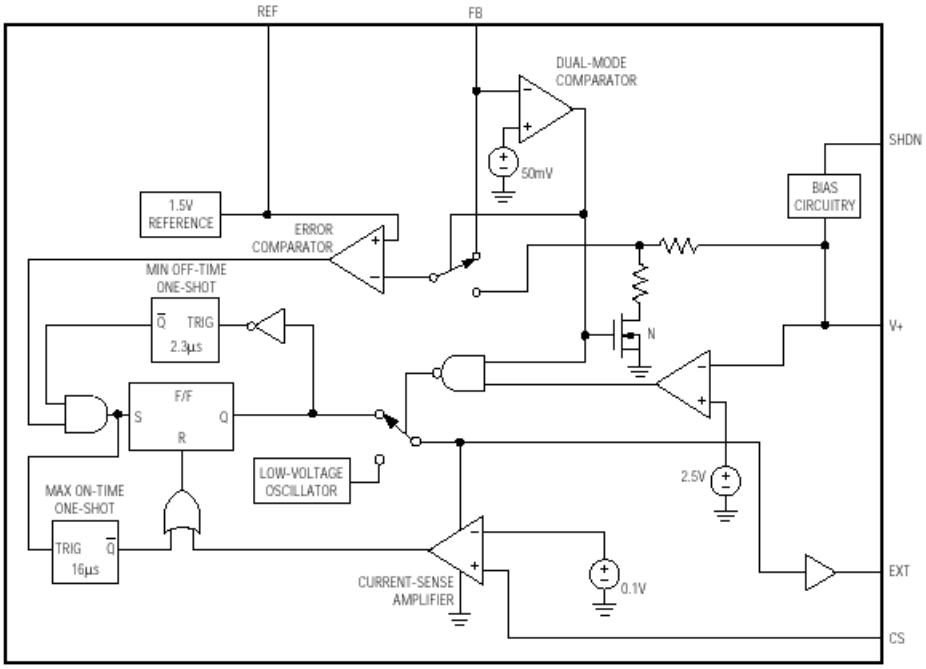


Fig. 4.1 Functional diagram for MAX1771 step-up converter

PIN	NAME	FUNCTION
1	EXT	Gate Drive for External N-Channel Power Transistor
2	V+	Power-Supply Input. Also acts as a voltage-sense point when in bootstrapped mode. Connected to ground for normal operation
3	FB	Feedback Input for Adjustable-Output Operation
4	SHDN	Active-High TTL/CMOS Logic-Level Shutdown Input. Connected to ground for normal operation
5	REF	1.5V Reference Output that can source 100mA for external loads. The reference is disabled in shutdown
6	AGND	Analog Ground
7	GND	High-Current Ground Return for the Output Driver
8	CS	Positive Input to the Current-Sense Amplifier

Table 4.1 Pin configuration for step-up converter

In bootstrapped mode, the IC is powered from the output (V_{OUT}, which is connected to V+) and the input voltage range is 2V to V_{OUT}. The voltage applied to the gate of the external power transistor is switched from V_{OUT} to ground, providing more switch gate drive and thus reducing the transistor's on-resistance. In non-bootstrapped mode, the IC is powered from the input voltage (V+) and operates with minimum supply current. In this mode, FB is the output voltage sense point. Since the voltage swing applied to the gate of the external power transistor is reduced (the gate swings from V+ to ground), the power transistor's on-resistance increases at low input voltages. However, the supply current is also reduced because V+ is at a lower voltage, and because less energy is consumed while charging and discharging the external MOSFET's gate capacitance. The

minimum input voltage is 3V when using external feedback resistors. With supply voltages below 5V, bootstrapped mode is recommended. For the current application, the driver is supplied in bootstrapped mode.

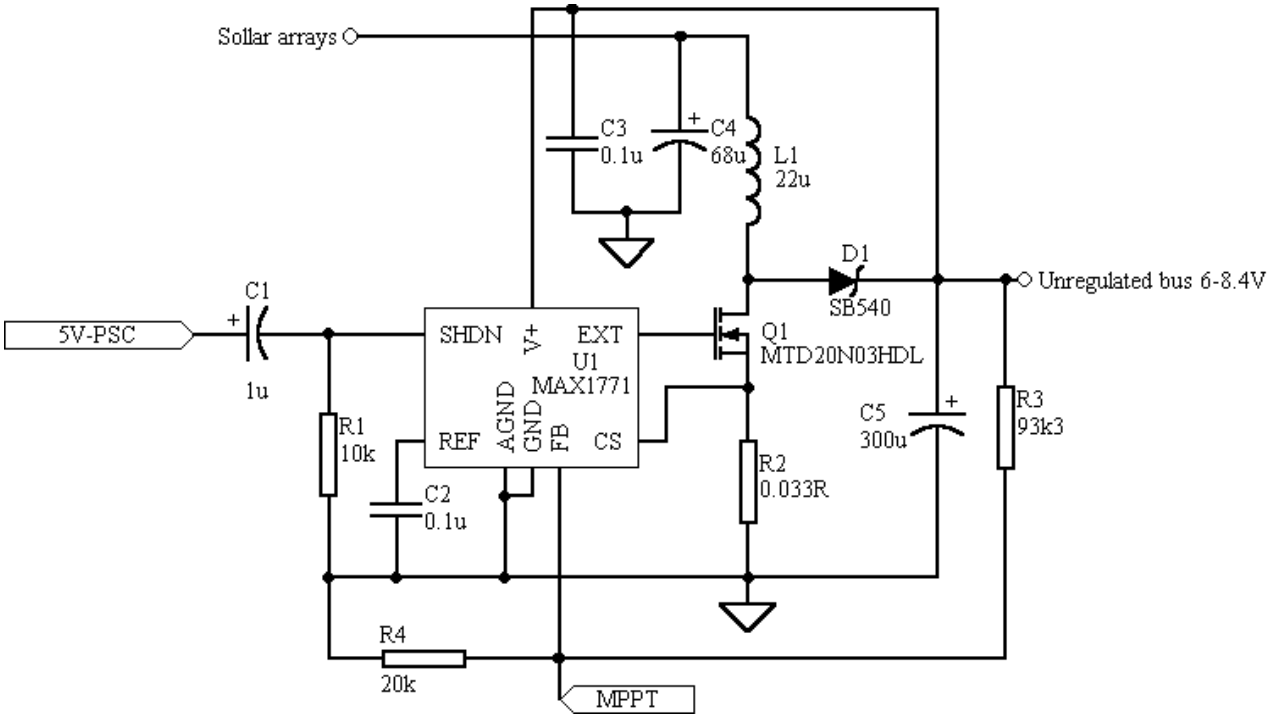


Figure 4.2 Scheme of application for the step-up converter MAX1771

Choose of external components

- **Setting the output voltage (Unregulated Bus 6-8.4V)**

To set the output voltage, first determine the mode of operation, either bootstrapped or non-bootstrapped. Bootstrapped mode provides more output current capability, while non-bootstrapped mode reduces the supply current.

The MAX1771's output voltage can be adjusted from very high voltages down to 3V, using external resistors R_3 and R_4 configured as voltage divider. For adjustable-output operation, the feedback resistor R_4 should be selected in the 10kΩ to 500kΩ range. R_3 is given by:

$$R_3 = R_4 \cdot \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{4.1}$$

where V_{REF} equals 1.5V. If R_4 is chosen to have 20kΩ and U_{OUT} equals with 8.4V it occurs:

$$R_3 = 20 \cdot 10^3 \cdot \left(\frac{8.4}{1.5} - 1 \right) = 93.3k\Omega \tag{4.2}$$

Considering that the batteries are using their protection circuits is not needed a too precise voltage regulation.

The voltage on the FB pin will be regulated externally using three different types of inputs: a fixed one using a voltage divider, the output of battery charger and MPPT circuitry ADP3810AR-8.4 and the digital MPPT programmed in the MCU. These three inputs are selectable using a multiplexer.

- **Determining R_{SENSE} (R_2)**

To select R_{SENSE} theoretical output current curves shown in datasheet (figure 4.3) have been used. They were derived using the minimum (worst-case) current-limit comparator threshold value over the extended temperature range (-40°C to +85°C). No tolerance was included for R_{SENSE}. The voltage drop across the diode was assumed to be 0.5V, and the drop across the power switch $r_{DS(ON)}$ and coil resistance was assumed to be 0.3V.

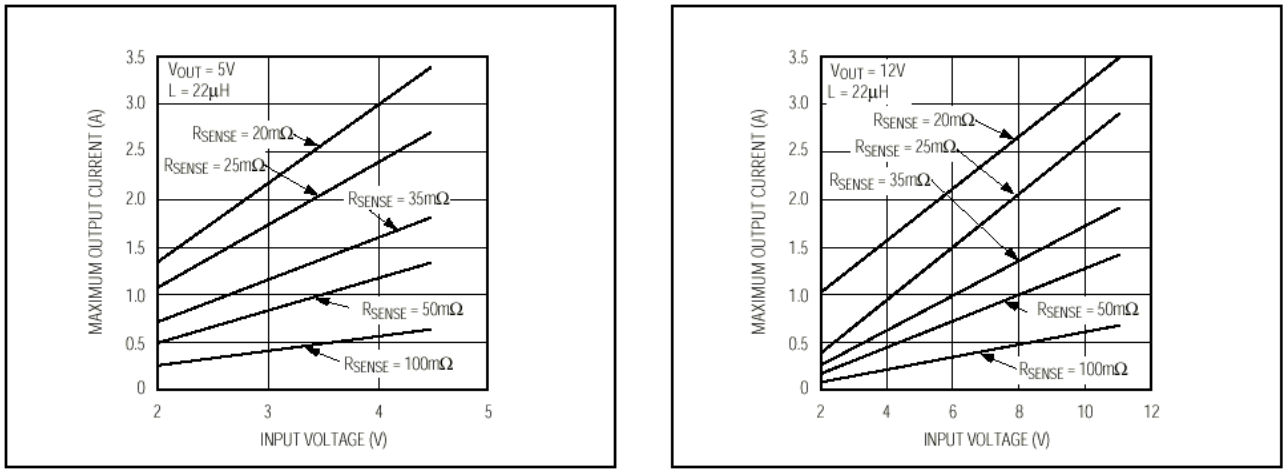


Figure 4.3 Maximum Output Current vs. Input voltage for V_{OUT} equal with 5V and 12V

Considering the curves from the figure 4.3 and the standardized values for shunt resistors, R_{SENSE} (R_2) was chosen to be 0.033Ω.

- **Determining the inductor (L)**

Practical inductor values range is from 10µH to 300µH. 22µH is a good choice for most applications. In applications with large input/output differentials, the IC's output current capability will be much less when the inductance value is too low, because the IC will always operate in discontinuous mode. If the inductor value is too low, the current will ramp up to a high level before the current-limit comparator can turn off the switch.

The minimum on-time for the switch ($t_{ON(\min)}$) is approximately 2µs; the inductor should be selected to allow the current to ramp up to I_{LIM}.

Standard operating circuits are using a 22µH inductor. If a different inductance value is desired, the inductor L will be selected such that:

$$L \geq \frac{V_{IN}(\max) \cdot 2\mu s}{I_{LIM}} \tag{4.3}$$

Considering that $V_{IN(\max)}$ is 5V and I_{LIM} equals with 1A results:

$$L \geq \frac{5(V) \cdot 2(\mu s)}{1(A)} \quad \Rightarrow \quad L \geq 10(\mu H) \tag{4.4}$$

The value for the inductor was chosen as being the same value indicated by the manufacturer of the device, in the datasheet, respectively 22μH.

Larger inductance values tend to increase the start-up time slightly, while smaller inductance values allow the coil current to ramp up to higher levels before the switch turns off, increasing the ripple at light loads. Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. It should be ensured that the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current rating set by R_{SENSE}. However, it is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, is to be used a coil with low DC resistance, preferably under 20mΩ. To minimize radiated noise, will be used a toroid, a pot core, or a shielded coil.

- **Power Transistor Selection**

For selection of the N-FET, three important parameters are: the total gate charge (Q_g), on-resistance ($r_{DS(ON)}$), and reverse transfer capacitance (C_{RSS}).

Q_g takes into account all capacitances associated with charging the gate. The typical Q_g has to be used value for best results; the maximum value is usually grossly over-specified since it is a guaranteed limit and not the measured value. The typical total gate charge should be 50nC or less. With larger numbers, the EXT pins may not be able to adequately drive the gate. The EXT rise/fall time varies with different capacitive loads as shown in the datasheet, Typical Operating Characteristics section.

The two most significant losses contributing to the N-FET's power dissipation are I^2R losses and switching losses. The transistor should be selected with low $r_{DS(ON)}$ and low C_{RSS} to minimize these losses.

The maximum required gate-drive current is determined from the Q_g specification in the N-FET data sheet. The MAX1771's maximum allowed switching frequency during normal operation is 300kHz; but at start-up, the maximum frequency can be 500kHz, so the maximum current required to charge the N-FET's gate is $f_{(\max)} \cdot Q_{g(typ)}$.

For the MTD20N03HDL transistor, from the data sheet, the typical Q_g number is 13.4nC (for V_{GS}=5V). Therefore the current required to charge the gate is:

$$I_{GATE} = f_{(\max)} \cdot Q_g = 500[\text{kHz}] \cdot 13.4[\text{nC}] = 6.7[\text{mA}] \tag{4.5}$$

The bypass capacitor on $V+$ (C_3) must instantaneously furnish the gate charge without excessive droop (imposed less than 200mV):

$$\Delta V+ = \frac{Q_g}{C_3} = \frac{13.4[\text{nC}]}{0.1[\mu\text{F}]} = 134[\text{mV}] \tag{4.6}$$

The transistor recommended in the datasheet for MAX1771 is MTD20N03. The N-channel MOSFET chosen for the application has 20A continuous drain current and 30V drain-source voltage. Also, is required an on-resistance as small as possible. The $R_{DS(on)}$ of this device is 35mΩ.

- **Diode**

The MAX1771's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended with average current rating exceeding the peak current limit set by R_{SENSE}, and that break-down voltage exceeding V_{OUT}. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantages of its high leakage current. Taking in consideration all of this, the diode chosen for this application is SB540 with $I_{F(AV)}$ = 5A, V_{RRM} = 40V and V_{RMS} = 28V.

- **Capacitor Selection**

Output Filter Capacitor (C_5)

The primary criterion for selecting the output filter capacitor (C_5) is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the ripple seen on the output voltage. Smaller-value and/or higher-ESR capacitors are acceptable for light loads or in applications that can tolerate higher output ripple. Since the output filter capacitor's ESR affects efficiency, low-ESR capacitors will be used for best performance. For reducing ESR is also possible to connect few capacitors in parallel.

The manufacturer is indicating for the applications like the presented one an output capacitor of 300µF. For reducing ESR of the output capacitor, will be used three capacitors of 100µF connected in parallel.

Input Bypass Capacitors (C_4)

The input bypass capacitor (C_4) reduces peak currents drawn from the voltage source and also reduces noise at the voltage source caused by the switching action of the MAX1771. The input voltage source impedance determines the size of the capacitor required at the $V+$ input. As with the

output filter capacitor, a low-ESR capacitor is recommended. For output currents up to 1A, 68µF (C_4) is adequate, although smaller bypass capacitors may also be acceptable.

The IC is bypassed with a 0.1µF ceramic capacitor (C_3) placed as close to the *V*+ and GND pins as possible.

Reference Capacitor

REF pin is bypassed with a 0.1µF capacitor (C_2). REF can source up to 100µA of current for external loads. This reference is not used in present application.

Feed-Forward Capacitor

In adjustable output voltage and non-bootstrapped modes, parallel a 47pF to 220pF capacitor across R_2. The capacitor should have the lowest value that insures stability; high capacitance values may degrade line regulation. For this reason this capacitor has a value of 100pF.

- **Choosing the components for timed start-up**

After the kill switch is released (launch procedure) the step-up converter should start after a short period. For this reason a timer is used on the SHDN pin. Basically is an *RC* network formed from R_1 and C_1 (see figure 4.2) circuit which is keeping this input high for a period equal with the time constant of *RC* network.

For the chosen components R_1=10kΩ and C_1=1µF the time constant will be:

4.2.1. Battery charger circuitry and MPPT

The ADP3810 battery charger combines a programmable current limit with a battery voltage limit to provide a constant current, constant voltage battery charger controller. The circuitry includes two gain stages (GM), a precision 2.0V reference, a control input buffer, an Undervoltage Lock Out (UVLO) comparator, an output buffer and an over-voltage comparator.

The ADP3810 has internal thin-film resistors that are trimmed to provide a precise final voltage for LiIon batteries. Four voltage options are available, corresponding to 1-4 LiIon cells as follows: 4.2V, 8.4V, 12.6V and 16.8V.

Here are a few features of the ADP3810 circuit:

- Programmable charge current
- High precision battery voltage limit
- Precision 2.000V reference
- Low voltage drop current sense: 300mV full scale
- Full operation in shorted and open battery conditions

- Wide operating supply range: 2.7V to 16V
- Undervoltage lockout

A functional block diagram of the circuit is presented in figure 4.2.

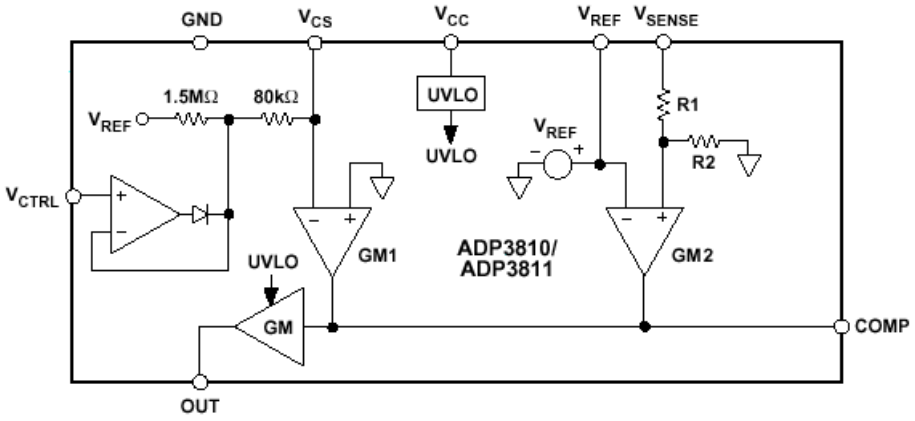


Figure 4.4 Simplified functional block diagram for battery charger

Pin Description

Pin	Name	Description
1	V_{SENSE}	Battery Voltage Sense Input.
2	V_{CS}	Current Sense Input.
3	COMP	External Compensation Pin.
4	OUT	Optocoupler Current Output Drive.
5	V_{CTRL}	DC Control Input to Set Current Limit, 0 V to 1.2 V.
6	GND	Ground Pin.
7	V_{REF}	Reference Output. Nominally 2.0 V.
8	V_{CC}	Positive Supply.

The ADP3810 contain the following blocks (shown in Figure 4.4):

- Two "GM" type error amplifiers control the current loop (GM1) and the voltage loop (GM2).
- A common COMP node is shared by both GM amplifiers such that an RC network at this node helps compensate both control loops.
- A precision 2.0V reference is used internally and is available externally for use by other circuitry. The 0.1µF bypass capacitor shown is required for stability.
- A current limited buffer stage (GM3) provides a current output, I_{OUT}, to control an external dc-dc converter. The dc-dc converter must have a control scheme such that higher I_{OUT} results in lower duty cycle. If this is not the case, a simple, single transistor inverter can be used for control phase inversion.
- An amplifier buffers the charge current programming voltage, V_{CTRL} , to provide a high impedance input.

- An UVLO circuit shuts down the GM amplifiers and the output when the supply voltage (V_{CC}) falls below 2.7V. This protects the charging system from indeterminate operation.
- A transient overshoot comparator quickly increases I_{OUT} when the voltage on the "+" input of GM2 rises over 120mV above V_{REF}. This clamp shuts down the dc-dc converter to quickly recover from overvoltage transients and protect external circuitry.

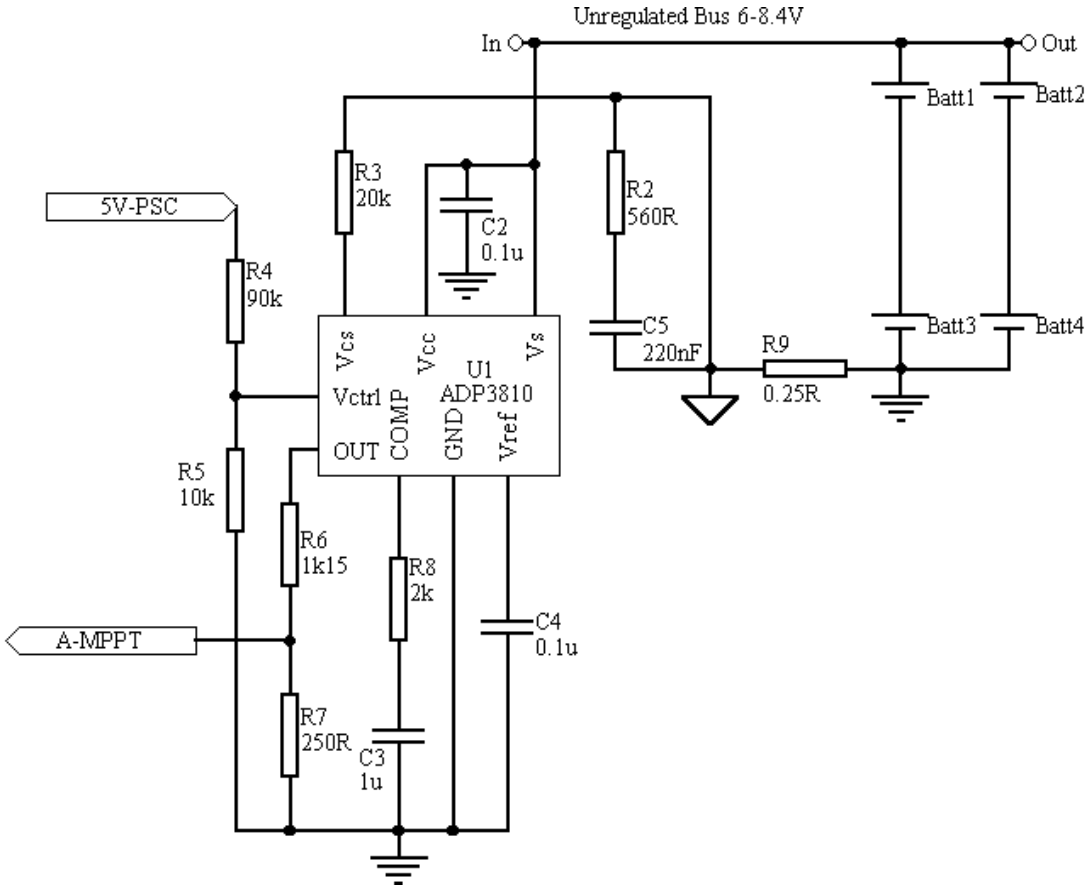


Figure 4.5 Application scheme for Battery Charger ADP3810

Functional description

The current limit amplifier senses the voltage drop across an external sense resistor to control the average current for charging a battery. The voltage drop can be adjusted from 25mV to 300mV, giving a charging current limit from 100mA to 1.2A with a 0.25Ω sense resistor. An external dc voltage on the V_{CTRL} input sets the voltage drop. As the battery voltage approaches its voltage limit, the voltage sense amplifier takes over to maintain a constant battery voltage. The two amplifiers essentially operate in an "OR" fashion. Either the current is limited, or the voltage is limited.

Description of Battery Charging Operation

The IC based system shown in figure 4.5 charges a battery with a dc current supplied by a dc-dc converter, which is most likely a switching type supply but could also be a linear supply

where feasible. The value of the charge current is controlled by the feedback loop comprised of R_3, R_2, GM1, the external dc-dc converter and a dc voltage at the V_{CTRL} input. The actual charge current is set by the voltage, V_{CTRL}, and is dependent upon the choice for the values of R_3 and R_2 according to the formula below:

$$I_{CHARGE} = \frac{1}{R_3} \cdot \frac{R_2}{80k\Omega} \cdot V_{CTRL} \tag{4.8}$$

Typical values are $R_3 = 0.25\Omega$ and $R_2 = 20k\Omega$, which result in a charge current of 0.5A for a control voltage of 0.5V. The 80kΩ resistor is internal to the IC, and it is trimmed to its absolute value. The positive input of GM1 is referenced to ground, forcing the V_{CS} pin to a virtual ground. The resistor R_3 converts the charge current into the voltage at V_{RCS} , and it is this voltage that GM1 is regulating. The voltage at V_{RCS} is equal to $-(R_3/80k\Omega)$ V_{CTRL}. When V_{CTRL} equals 1.0V, V_{RCS} equals –250mV. If V_{RCS} falls below its programmed level (i.e., the charge current increases), the negative input of GM1 goes slightly below ground. This causes the output of GM1 to source more current and drive the COMP node high, which forces the current, I_{OUT}, to increase. A higher I_{OUT} decreases the drive to the dc-dc converter, reducing the charging current and balancing the feedback loop. As the battery approaches its final charge voltage, the voltage loop takes over. The system becomes a voltage source, floating the battery at constant voltage thereby preventing overcharging. The constant voltage feature also protects the circuitry that is actually powered by the battery from overvoltage if the battery is removed. The voltage loop is comprised of R_1, R_2, GM2 (see figure 4.5) and the dc-dc converter. The final battery voltage is simply set by the ratio of R_1 and R_2 according to the following equation ($V_{REF} = 2V$):

$$V_{BATT} = 2[\mathrm{V}] \cdot \left(\frac{R_1}{R_2} + 1 \right) \tag{4.9}$$

If the battery voltage rises above its programmed voltage, V_{SENSE} is pulled above V_{REF}. This causes GM2 to source more current, raising the COMP node voltage and I_{OUT}. As with the current loop, the higher I_{OUT} reduces the duty cycle of the dc-dc converter and causes the battery voltage to fall, balancing the feedback loop.

Charge Termination

If the system is charging a LiIon battery, the main criteria to determine charge termination is the absolute battery voltage. The ADP3810, with its accurate reference and internal resistors, accomplishes this task. The ADP3810's guaranteed accuracy specification of ±1% of the final battery voltage ensures that a LiIon battery will not be overcharged. This is especially important with LiIon batteries because overcharging can lead to catastrophic failure. It is also important to

insure that the battery be charged to a voltage equal to its optimal final voltage (typically 4.2V per cell). Stopping at less than 1% of full-scale results in a battery that has not been charged to its full mAh capacity, reducing the battery's run time and the end equipment's operating time.

V_{CTRL} Input and Charge Current Programming Range

The voltage on the V_{CTRL} input determines the charge current level. This input is buffered by an internal single supply amplifier (labeled BUFFER) to allow easy programmability of V_{CTRL}. The guaranteed input voltage range of the buffer is from 0.0V to 1.2 V. Considering the input power from solar arrays, V_{CTRL} voltage is fixed at 0.5V using a voltage divider and a external 5V power supply, the same power supply used for all the power supply circuits, as in figure below.

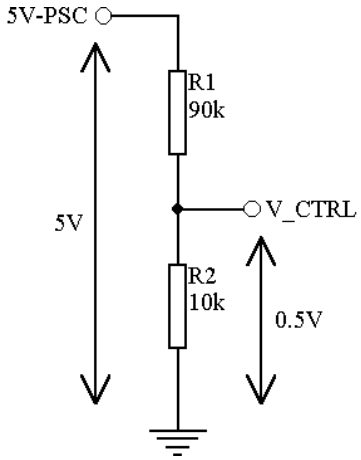


Figure 4.6 Set of V_{CTRL} value

$$U_{OUT} = \frac{R_2}{R_1 + R_2} \cdot U_{IN} \tag{4.10}$$

When V_{CTRL} is in the range of 0.0V to 0.5V, the output of the internal amplifier is fixed at 0.5V. This corresponds to a charge current of 500mA for $R_3 = 0.25\Omega$, $R_2 = 20\ k\Omega$.

V_{REF} Output

The internal band gap reference is not only used internally for the voltage and current loops, but it is also available externally if an accurate voltage is needed. The reference employs a pnp output transistor for low dropout operation. The reference is guaranteed to source 5mA with a dropout voltage of 400mV or less. The 0.1μF capacitor on the reference pin is integral in the compensation of the reference and is therefore required for stable operation. If desired, a larger value of capacitance can also be used for the application, but a smaller value should not be used. This capacitor should be located close to the V_{REF} pin.

Output Stage

The output stage performs two important functions. It is a buffer for the compensation node, and as such, it has a high impedance input. It is also a GM stage. The gain from the COMP node to the OUT pin is approximately 5mA/V. With a load resistor of 1 kΩ, the voltage gain is equal to five as specified in the data sheet. A different load resistor results in a gain equal to $R_L \cdot (5mA/V)$. The guaranteed output current is 5mA, which is much more than the typical 1mA to 2mA required in most applications.

Current Loop Accuracy Considerations

The accuracy of the current loop is dependent on several factors such as the offset of GM1, the offset of the V_{CTRL} buffer, the ratio of the internal 80kΩ compared to the external 20kΩ resistor, and the accuracy of R_3 . The specification for current loop accuracy states that the full-scale current sense voltage, V_{RCS}, of –300 mV is guaranteed to be within 15mV of this value. This assumes an exact 20kΩ resistor for R_2. Any errors in this resistor will result in further errors in the charge current value. For example, a 5% error in resistor value will add a 5% error to the charge current. The same is true for R_3, the current sense resistor. Thus, 1% or better resistors are recommended.

Voltage Loop Accuracy Considerations

The accuracy of the voltage loop is dependent on the offset of GM2, the accuracy of the reference voltage, the bias current of GM2 through R_1 and R_2, and the ratio of R_1/R_2. For the demanding application of charging LiIon batteries, the accuracy of the ADP3810 is specified with respect to the final battery voltage. This is tested in a full feedback loop so that the single accuracy specification given in the specification table accounts for all of the errors mentioned above.

STABILIZATION OF FEEDBACK LOOPS

The ADP3810 uses two transconductance error amplifiers with “merged” output stages to create a shared compensation point (COMP) for both the current and voltage loops as explained previously. Since the voltage and current loops have significantly different natural crossover frequencies in a battery charger application, the two loops need different inverted zero feedback loop compensations that can be accomplished by two series *RC* networks. One provides the needed low frequency (typical f_C<100Hz) compensation to the voltage loop, and the other provides a separate high frequency (f_C~1kHz–10kHz) compensation to the current loop. In addition, the current loop input requires a ripple reduction filter on the V_{CS} pin to filter out switching noise. Instead of placing both *RC* networks on the COMP pin, the current loop network is placed between V_{CS} and ground as shown in figure 4.5 (C_5 and R_2). Thus, it performs two functions, ripple reduction and loop compensation.

Loop Stability Criteria

1. The voltage loop has to be stable when the battery is floating.
2. The current loop has to be stable when the battery is being charged within its specified charge current range.
3. Both loops have to be stable within the specified input source voltage range.

4.3. Battery protection circuit

The batteries are provided a protection circuit for overcharging and overdischarging. In order to perform this function, the UCC3911 IC from Texas Instruments has been chosen. This device is able to ensure protection for a string of two series connected Li-Ion cells.

The UCC3911 is a two-cell lithium-ion (Li-Ion) and lithium-polymer (Li-Poly) battery pack protector device that incorporates an on-chip series FET switch thus reducing manufacturing costs and increasing reliability. The device's primary function is to protect both Li-Ion and Li-Poly cells in a two-cell battery pack from being either overcharged (overvoltage) or overdischarged (undervoltage). It employs a precision bandgap voltage reference that is used to detect when either cell is approaching an overvoltage or undervoltage state. When on-board logic detects either condition, the series FET switch opens to protect the cells. Principal characteristics of this IC are:

- provides protection against battery pack output shortcircuit
- extremely low power drain on batteries of about 20 μA
- used for two-cell battery packs
- low internal FET switch voltage drop
- user controllable delay for tripping short
- 3 A current capacity

A functional diagram for the device can be seen in figure 4.7. and a detailed pin description for the device is given in Table 4.2.

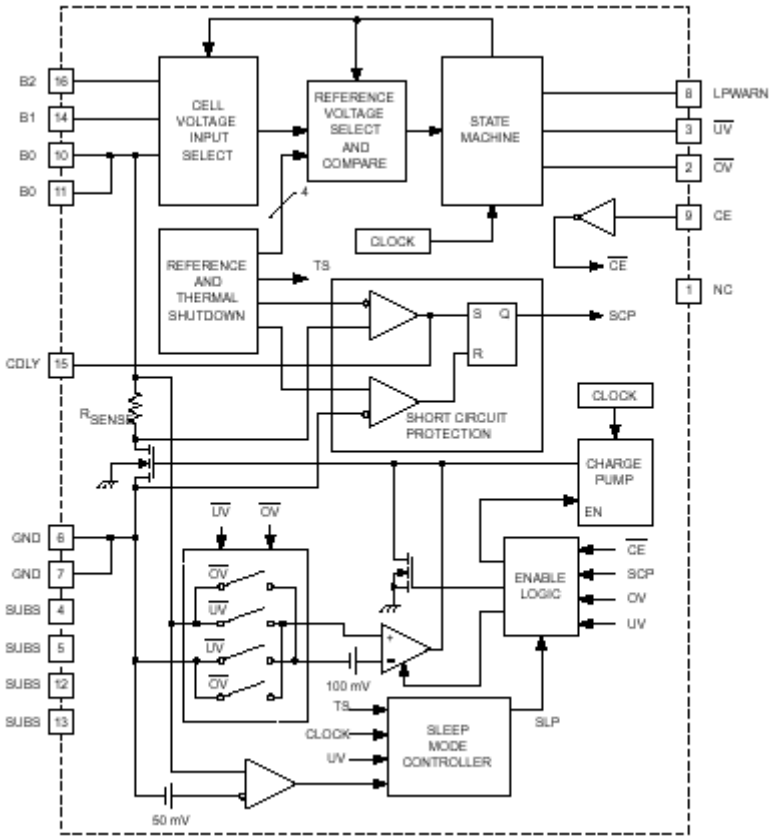


Figure 4.7 Functional diagram for battery protection circuit UCC3911

TERMINAL		I/O	DESCRIPTION
NAME	PACKAGE DP		
B0	10, 11	I	Connects to the negative terminal of the lower cell in the battery pack
B1	14	I	Connects to the junction of the positive terminal of the lower cell and the negative terminal of the upper cell in the battery pack
B2	16	I	Connects to the positive terminal of the upper cell in the battery pack. This pin also connects to the positive of the two terminals that are presented to the user of the battery pack
CDLY	15	I	Delay control pin for the short circuit protection feature
CE	9	O	Chip enable. The internal FET is disabled when CE is connected to B0
GND	6,7	–	In an overcharged state, current is allowed to flow only into this terminal. Similarly, in an over-discharged state, current is allowed to flow only out of this terminal
LPWARN	8	O	This active–high signal is the low Power Warning. The voltage on this pin goes high (to B2 potential) as soon as either of the battery's cells voltage falls below 3.0 V. Once the UV state is entered, this output goes back to low

$\overline{OV}$	2	O	This active–low signal indicates the state of the state machine's $\overline{OV}$ bit. When low, it indicates that one or both cells are overvoltage. Further charging is inhibited by the opening of the FET switch
SUBS	4,5,12,13	I	The substrate connections connect these points to a heat sink which is electrically isolated from all other device pins
$\overline{UV}$	3	O	This active–low signal indicates the state of the state machine's undervoltage bit. When low, it indicates that one or both cells are under voltage. Further discharging is inhibited by the opening of the FET switch

Table 4.2 Pin description for UCC3911

A negative feedback loop controls the FET switch when the battery pack is in either the overvoltage or undervoltage state. In the overvoltage state the action of the feedback loop is to allow only discharge current to pass through the FET switch. In the undervoltage state, only charging current is allowed to flow. The operational amplifier that drives the loop is powered only when in one of these two states. In the undervoltage state the chip enters sleep mode until it senses that the pack is being charged. The FET switch is driven by a charge pump when the battery pack is in a normally charged state to achieve the lowest possible $R_{DS(on)}$. In this state the negative feedback loop's operational amplifier is powered down to conserve battery power. Short circuit protection for the battery pack is provided and has a nominal delay of 100 μs before tripping.

An external capacitor may be connected between CDLY and B0 to increase this delay time to allow longer overcurrent transients. A chip enable (CE) pin is provided that when held low, inhibits normal operation of the device to facilitate assembly of the battery pack.

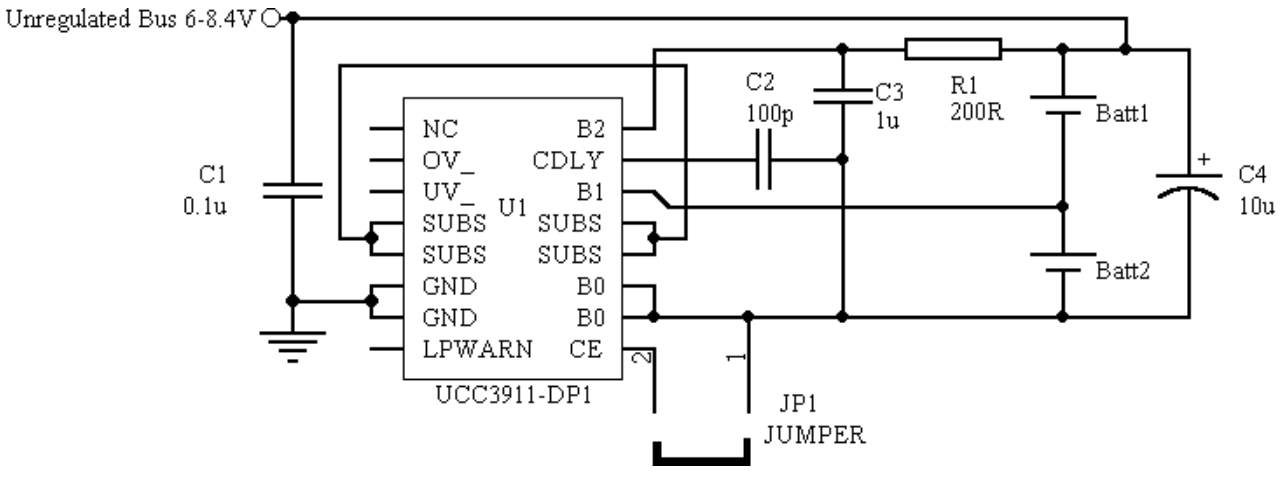


Figure 4.8 Scheme of application for battery protection circuit

Short-circuit protection

The demands of true short-circuit protection require that careful attention be paid to the selection of a few external components. In the application circuit shown in figure 4.8, C_1 protects

the battery pack output terminals from inductive kick when the pack current is shut off due to an overcurrent or overvoltage/undervoltage condition. (It also increases the ESD protection level.)

The overcurrent delay capacitor (C_2), sets the time delay, after the overcurrent threshold is exceeded, before turning off the UCC3911's internal FET. If no capacitor is used, the nominal delay is 100µs. To charge large capacitive loads without tripping the overcurrent circuit, a small capacitor (typically less than 1000pF) is used to extend the delay time. The approximate delay time is given below and shown graphically in figure 4.9.

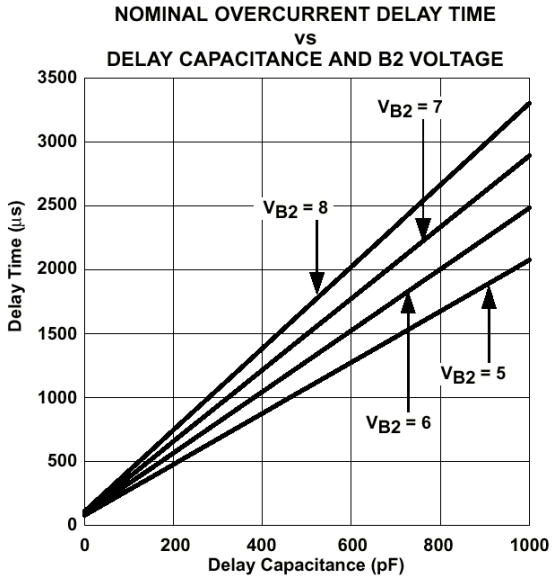


Figure 4.9 Nominal current delay time

$t_{DLY}[\mu s] = 25 + (25 + C_2[pF]) \cdot 0.4 \cdot V_{B2}$, therefore, for a capacitor C_2=100pF the minimum delay is:

$t_{DLY}(MIN) = 25 + (25 + 100) \cdot 0.4 \cdot 6 = 325[\mu s]$ when the battery voltage is minimum (6V) and the maximum delay:

$t_{DLY}(MAX) = 25 + (25 + 100) \cdot 0.4 \cdot 8.4 = 445[\mu s]$.

The amount of time required will be a function of the load capacitance, battery voltage, and the total circuit impedance, including the internal resistance of the cells, the UCC3911's on resistance, and the load capacitor ESR. The required delay time can be calculated from:

$$t = -R \cdot C \cdot \ln\left(\frac{I \cdot R}{V}\right) \tag{4.11}$$

In this equation, R is the total circuit resistance, C is the capacitor being charged, I is the overcurrent trip current (5.25A nominal), and V is the battery voltage. Using the minimum trip current of 3.5A and the maximum battery voltage of 8.4V, the worst case maximum delay time required is defined as:

$$t_{MAX}[\mu s] = -R \cdot C[\mu F] \cdot \ln\left(\frac{R}{2.4}\right) \tag{4.12}$$

Considering that C_{load} = 300μF, R = 0.2Ω (ESR from the capacitor added with resistance of the battery wires) it result:

$$t_{MAX} = -0.2 \cdot 300 \cdot \ln\left(\frac{0.2}{2.4}\right) = 149.094[\mu s] \tag{4.13}$$

To prevent a momentary cell voltage drop, caused by large capacitive loads, from causing an erroneous undervoltage shutdown, an *RC* filter is required in series with the two battery sense inputs, B1 and B2. If large capacitive loads (or other loads with surge currents above the overcurrent trip threshold) are not being applied to the pack terminals, the overcurrent delay time can be short and for B1 input the filter is not needed. In addition, the time constant of R_1 and C_3 (filter for B2 input) can be made much shorter. R_1 and C_3 are still necessary, however, to assure proper operation under short circuit conditions. It is important to maintain a minimum R_1/C_3 time constant of 100 μs.

If it is selected a time constant of 200μs, $\tau_{R1C3} = R_1 \cdot C_3 = 220[\mu s]$, it yields to R_1 = 200Ω and C_3 = 1μF.

Capacitor C_4 is recommended, in case the wires connecting to the top and bottom of the cell stack are more than an inch long (not likely in a small battery pack). In this case, a 10μF, low ESR capacitor is recommended to prevent excessive overshoot at turn-off due to wiring inductance.

4.4. Converter for the 5 V bus

For the 5V bus a step-down converter is to be used. The MAX174X family of ICs are step-down DC-DC controllers capable of handling up to 36V inputs. The MAX1744 device has been chosen because the output voltage is presetable for 5V. The main characteristics of this converter are:

- High-Voltage Operation (up to 36V IN)
- Efficiency >90%
- Output Power Capability Exceeds 50W
- 10-Pin μMax Package
- Low-Dropout Voltage

- 100% (max) Duty Cycle
- 90µA Quiescent Current
- 4µA Shutdown Current
- Up to 330kHz Switching Frequency
- Output Voltage
- 5V or 3.3V (MAX1744)
- Adjustable 1.25V to 18V (MAX1745)
- Current-Limited Control Scheme

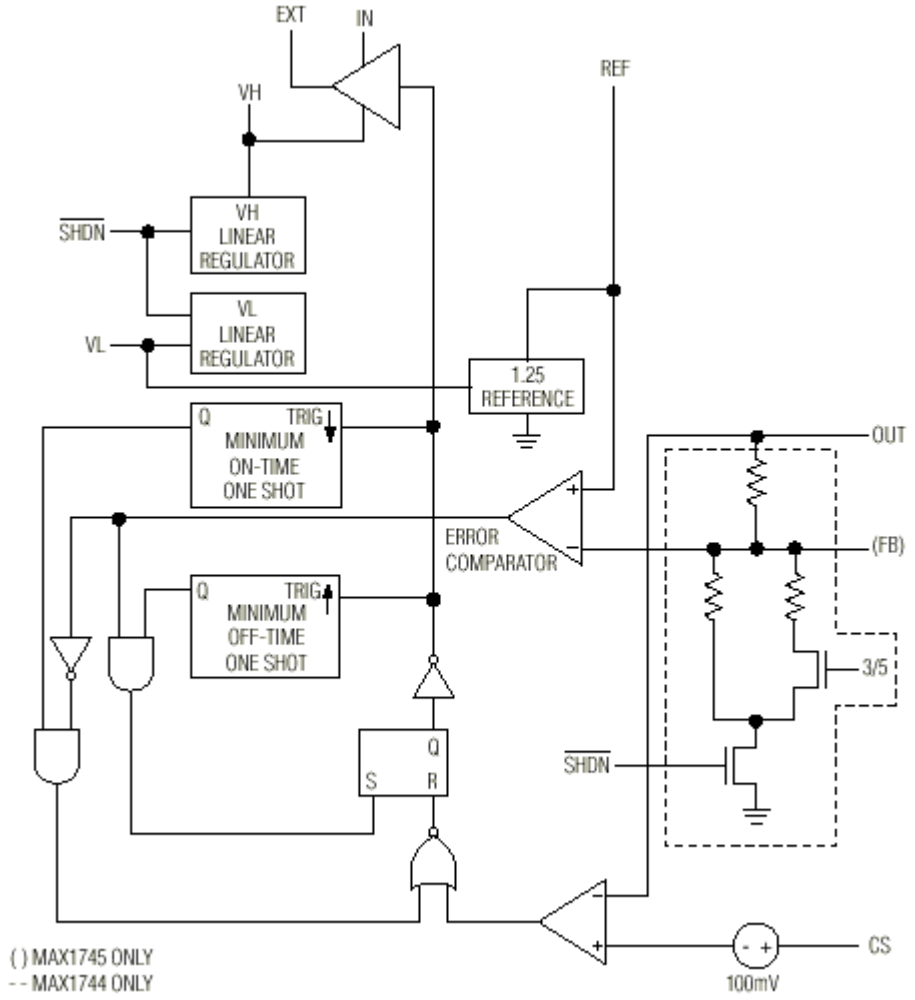


Figure 4.10 Functional diagram for step-up converter MAX1744

This part is using a proprietary current-limited control scheme for excellent light and full-load efficiency, while their 330kHz (max) switching frequency permits small external components for space-critical applications. Operation to 100% duty cycle permits the lowest possible dropout voltage. The MAX1744 contains an internal feedback network that provides a pin-selectable output voltage of either 3.3V or 5V.

Pin Description

PIN	PIN NAME	FUNCTION
1	GND	Ground
2	VL	Linear Regulator Output. VL provides power to the internal circuitry and can supply up to 1mA to an external load. Bypass VL to GND with 4.7uF or greater capacitor.
3	REF	1.25V Reference Output. REF can supply up to 100A to an external load. Bypass REF to GND with a 0.1uF or greater ceramic capacitor.
4	3/5	3.3V or 5V Selection. Connect 3/5 to GND to set the output voltage to 3.3V. Connect 3/5 to VL to set the output voltage to 5V.
5	OUT	Sense Input for Fixed 5V or 3.3V Output Operation (MAX1744) and Negative Current-Sense Input (MAX1744/5). OUT is connected to an internal voltage-divider (MAX1744). OUT does not supply current.
6	CS	Current-Sense Input. Connect the current-sense resistor between CS and OUT. External MOSFET is turned off when the voltage across the resistor is equal to or greater than the current limit trip level (100mV).
7	$\overline{SHDN}$	Active-Low Shutdown Input. Connect $\overline{SHDN}$ to IN for normal operation. Drive $\overline{SHDN}$ to low to shut the part off. In shutdown mode, the reference, output, external MOSFET, and internal regulators are turned off.
8	VH	High-Side Linear Regulator Output. VH provides a regulated output voltage that is 5V below IN. The external P-channel MOSFET gate is driven between IN and VH. Bypass VH to IN with a 4.7uF or greater capacitor (see Capacitor Selection).
9	EXT	Gate Drive for External P-Channel MOSFET. EXT swings between IN and VH.
10	IN	Positive Supply Input. Bypass IN to GND with a 0.47uF or greater ceramic capacitor.

The MAX1744 is high-voltage step-down DC-DC converter controller. These devices offer high efficiency over a wide range of input/output voltages and currents, making them optimal for use in applications such as telecom, automotive, and industrial control. Using an external P-channel MOSFET and current-sense resistor allows design flexibility and improved efficiency. The MAX1744 is automatically switching from PWM operation at medium and heavy loads to pulse-skipping operation at light loads to improve light-load efficiency. The low 90µA quiescent current further optimizes these parts for applications where low input current is critical. Operation to 100% duty cycle allows the lowest possible dropout voltage, which allows a wider input voltage variation. The small size, high switching frequency, and low parts count minimize the required circuit board area and component cost. figure 4.11 shows the MAX1744 typical application circuit.

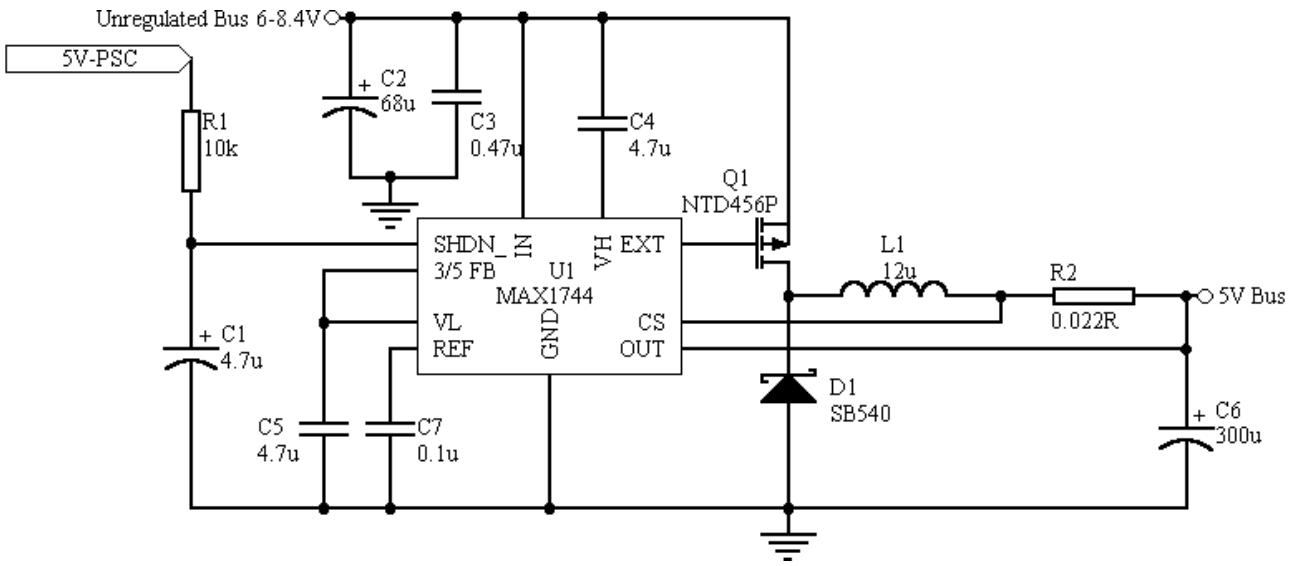


Figure 4.11 Application scheme for step-down converter MAX1744

Operating Modes

When delivering low output currents, the MAX1744 operate in discontinuous-conduction mode. Current through the inductor starts at zero, rises as high as the current limit, then ramps down to zero during each cycle. The switch waveform exhibits ringing, which occurs at the resonant frequency of the inductor and stray capacitance, due to residual energy trapped in the core when the commutation diode (D_1 in figure 4.11) turns off. When delivering medium-to-high output currents, the MAX1744 operate in PWM continuous-conduction mode. In this mode, current always flows through the inductor and never ramps to zero. The control circuit adjusts the switch duty cycle to maintain regulation without exceeding the peak switching current set by the current-sense resistor.

For the present application it can be considered that MAX1744 is operating in continuous-conduction mode.

Setting the Output Voltage

The MAX1744's output voltage can be selected to 3.3V or 5V under logic control by using the 3/5 pin. To ensure a 5V output the 3/5 pin is connected to VL.

VL Linear Regulator

The MAX1744 contains a 5V low-side linear regulator (VL) that powers the internal circuit and can supply up to 1mA to an external load. This allows the MAX1744 to operate up to 36V input, while maintaining low quiescent current and high switching frequency. When the input voltage goes below 5.5V, this regulator goes into dropout and the IN pin quiescent current will rise. VL should be bypassed with a 4.7µF or greater capacitor (C_5).

VH Linear Regulator

The MAX1744 is containing a high-side linear regulator (VH) that regulates its output to 5V below IN (the positive supply input voltage). This regulator limits the external P-channel MOSFET gate swing (EXT), allowing high input voltage operation without exceeding the MOSFET gate-source breakdown. VH is bypassed with a 4.7µF capacitor (C_4) between IN and VH.

Reference

The 1.25V reference is suitable for driving small external loads. It has a guaranteed 10mV maximum load regulation while sourcing load currents up to 100µA. The reference is turned off during shutdown. For normal operation the reference will be bypassed with 0.1µF (C_7). The bypass capacitor must be within 5mm of REF, with a direct trace to GND.

Current-Sense-Resistor Selection (R_2)

The current-sense comparator limits the peak switching current to V_{CS}/R_2, where R_2 is the value of the current-sense resistor and V_{CS} is the current-sense threshold. V_{CS} is typically 100mV. Minimizing the peak switching current will increase efficiency and reduce the size and cost of external components. However, since available output current is a function of the peak switching current, the peak current limit must not be set too low.

The peak current limit is set to 1.3 times the maximum load current by setting the current-sense resistor (R_2) to:

$$R_2 = \frac{V_{CS(MIN)}}{1.3 \cdot I_{OUT(MAX)}} \tag{4.14}$$

Considering the maximum output current as being 2A it yields to:

$$R_2 = \frac{0.085}{1.3 \cdot 2} = 0.0327\Omega \tag{4.15}$$

In concordance with standardized values for resistors R_2 was chosen to have 0.033Ω.

Inductor Selection

The essential parameters for inductor selection are inductance and current rating. The MAX1744 operate with a wide range of inductance values. In many applications, values between 4.7µH and 100µH take best advantage of the controller's high switching frequency.

The minimum inductance value is calculate as follows:

$$L_{(MIN)} = \frac{(V_{IN} - V_{OUT}) \cdot 1[\mu s]}{\frac{V_{CS(MIN)}}{R_2}} \tag{4.16}$$

where 1μs is the minimum on-time. Inductor values between 2 and 10 times $L_{(MIN)}$ are recommended. Therefore:

$$L_{(MIN)} = \frac{(8.4-5)\cdot 1}{\frac{0.085}{0.033}} = 1.32[\mu H] \tag{4.17}$$

and the final value for the inductance was chosen L = 12μH.

With high inductor values, the MAX1744 begin continuous-conduction operation at a lower fraction of the full load. The inductor's saturation and heating current ratings must be greater than the peak switching current to prevent overheating and core saturation. Saturation occurs when the inductor's magnetic flux density reaches the maximum level the core can support, and inductance starts to fall. The heating current rating is the maximum DC current the inductor can sustain without overheating. For optimum efficiency, the inductor winding's resistance should be less than the current-sense resistance.

External Switching Transistor

The MAX1744 drive a P-channel enhancement mode MOSFET. The EXT output swings from VH to IN. The MOSFET's on-resistance is should be specified for 5V gate drive or less.

Four important parameters for selecting a P-channel MOSFET are drain-to-source breakdown voltage, current rating, total gate charge (Q_g), and $R_{DS(ON)}$. The drain-to-source breakdown voltage rating should be at least a few volts higher than V_{IN}. The MOSFET should be chosen with a maximum continuous drain current rating higher than the peak current limit:

$$I_{D(MAX)} \geq I_{LIM(MAX)} \tag{4.18}$$

$$I_{LIM(MAX)} = \frac{V_{CS}}{R_2} = \frac{0.1}{0.033} = 3[A] \tag{4.19}$$

The Q_g specification should be 80nC or less to ensure fast drain voltage rise and fall times, and reduce power losses during transition through the linear region. Q_g specifies all of the capacitances associated with charging the MOSFET gate. $R_{DS(ON)}$ should be as low as practical to reduce power losses while the MOSFET is on. It should be equal to or less than the current-sense resistor.

Considering the specifications listed above, the MOSFET transistor selected for the application is NDT456P with the following specifications: drain-to-source breakdown voltage $V_{DSS} = -30V$, on-state drain current $I_D = -7.5A$, total gate charge $Q_g = 47nC$, and static drain-source on-resistance $R_{DS(ON)} = 0.041\Omega$ ($V_{GS} = -4.5V$, $V_{DS} = -5V$).

Diode Selection

The MAX1744's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5817–1N5822 family or surface-mount equivalents, are recommended. Ultra-high-speed rectifiers with reverse recovery times around 50ns or faster should be used for high output voltages, where the increased forward drop causes less efficiency degradation. Diode's peak current rating should exceed the peak current limit set by R_2, and that its breakdown voltage exceeds V_{IN}. Schottky diodes are preferred for heavy loads due to their low forward voltage, especially in low-voltage applications.

The diode selected for the application is SB540 with the following characteristics: average forward current $I_{F(AV)}$ = 5A, peak repetitive reverse voltage V_{RRM} = 40V and maximum RMS voltage V_{RMS} = 28V.

Capacitor Selection

The filter capacitors are chosen to service input and output peak currents with acceptable voltage ripple. ESR (Equivalent Series Resistance) in the output capacitor is a major contributor to output ripple, so low-ESR capacitors are recommended. Low-ESR tantalum, polymer, or ceramic capacitors are best. Low-ESR aluminum electrolytic capacitors are tolerable, but standard aluminum electrolytic capacitors are not recommended.

Voltage ripple is the sum of contributions from ESR and the capacitor value:

$$V_{RIPPLE} \approx V_{RIPPLE,ESR} + V_{RIPPLE,C} \tag{4.20}$$

For tantalum capacitors, the ripple is determined by the ESR, but for ceramic capacitors, the ripple is mostly due to the capacitance. Voltage ripple as a consequence of ESR is approximated by:

$$V_{RIPPLE,ESR} \approx (R_{ESR})\Delta I_{p-p} \tag{4.21}$$

The ripple due to the capacitance is approximately:

$$V_{RIPPLE,C} \approx \frac{L \cdot I_{PEAK}^2}{2 \cdot C \cdot V_O} \tag{4.22}$$

Estimation of the input (C_2) and output capacitor (C_6) values for given voltage ripple will be made as follows:

$$C_2 = \frac{\frac{1}{2} \cdot L_1 \cdot I_{\Delta L1}^2}{V_{RIPPLE,C3} \cdot V_{IN}} = \frac{\frac{1}{2} \cdot 12 \cdot 10^{-6} \cdot 2^2}{0.05 \cdot 8.4} = 57[\mu F] \tag{4.23}$$

$$C_6 = \frac{\frac{1}{2}\cdot L_1 \cdot I_{\Delta L1}^2}{V_{RIPPLE,C6}\cdot V_{OUT}}\cdot\left(\frac{V_{IN}}{V_{IN}-V_{OUT}}\right)=\frac{\frac{1}{2}\cdot 12\cdot 10^{-6}\cdot 2^2}{0.05\cdot 5}\cdot\left(\frac{8.4}{8.4-5}\right)=237.176[\mu F] \tag{4.24}$$

where $I_{\Delta L}$ is the change in inductor current and for continuous-conduction mode equals with output current and V_{RIPPLE} was chosen 50mV (1% from the output voltage). Considering the standardized values for capacitors, the chosen values for capacitors are $C_2 = 68\mu F$ and $C_6 = 300\mu F$.

These equations are suitable for initial capacitor selection; final values should be set by testing a prototype. Pursuing output ripple lower than the error comparator's hysteresis (0.6% of the output voltage) is not practical, since the MAX1744 will switch at slower frequencies, increasing inductor ripple current threshold. The output capacitor will be chosen with a working voltage rating higher than the output voltage.

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple at IN, caused by the circuit's switching action. It should be used a low-ESR capacitor. Two smaller-value low-ESR capacitors can be connected in parallel if necessary. The input capacitors should have the working voltage ratings higher than the maximum input voltage.

A surface-mount ceramic capacitor (C_3) will be placed very close to IN and GND. This capacitor bypasses the MAX1744, minimizing the effects of spikes and ringing on the power source (IN). The value for this capacitor is 0.47µF.

The REF pin is bypassed with 0.1µF (C_7). This capacitor should be placed within 5mm of the IC, next to REF, with a direct trace to GND.

Choosing the components for timed start-up

When the kill switch is released (launch procedure) the step-down converter should start in a short period after the step-up converter. For this reason a timer is used on the $\overline{SHDN}$ pin. Basically is an *RC* circuit, formed by R_1 and C_1 (see figure 4.11), circuit which is keeping this input low for a period equal with the time constant of the *RC* network.

For the chosen components $R_1 = 20k\Omega$ and $C_1 = 4.7\mu F$ the time constant will be:

$$\tau_{R1-C1} = R_1 \cdot C_1 = 20\cdot 10^3 \cdot 4.7\cdot 10^{-6} = 94[ms] \tag{4.25}$$

This time constant was chosen considering that this converter should start after the first converter is getting out from its transient domain.

4.5. Load protection circuits

Each user is using a protection circuit like in figure 4.12. The only difference between protections for different users is the current limit for power distribution switches TPS203x.

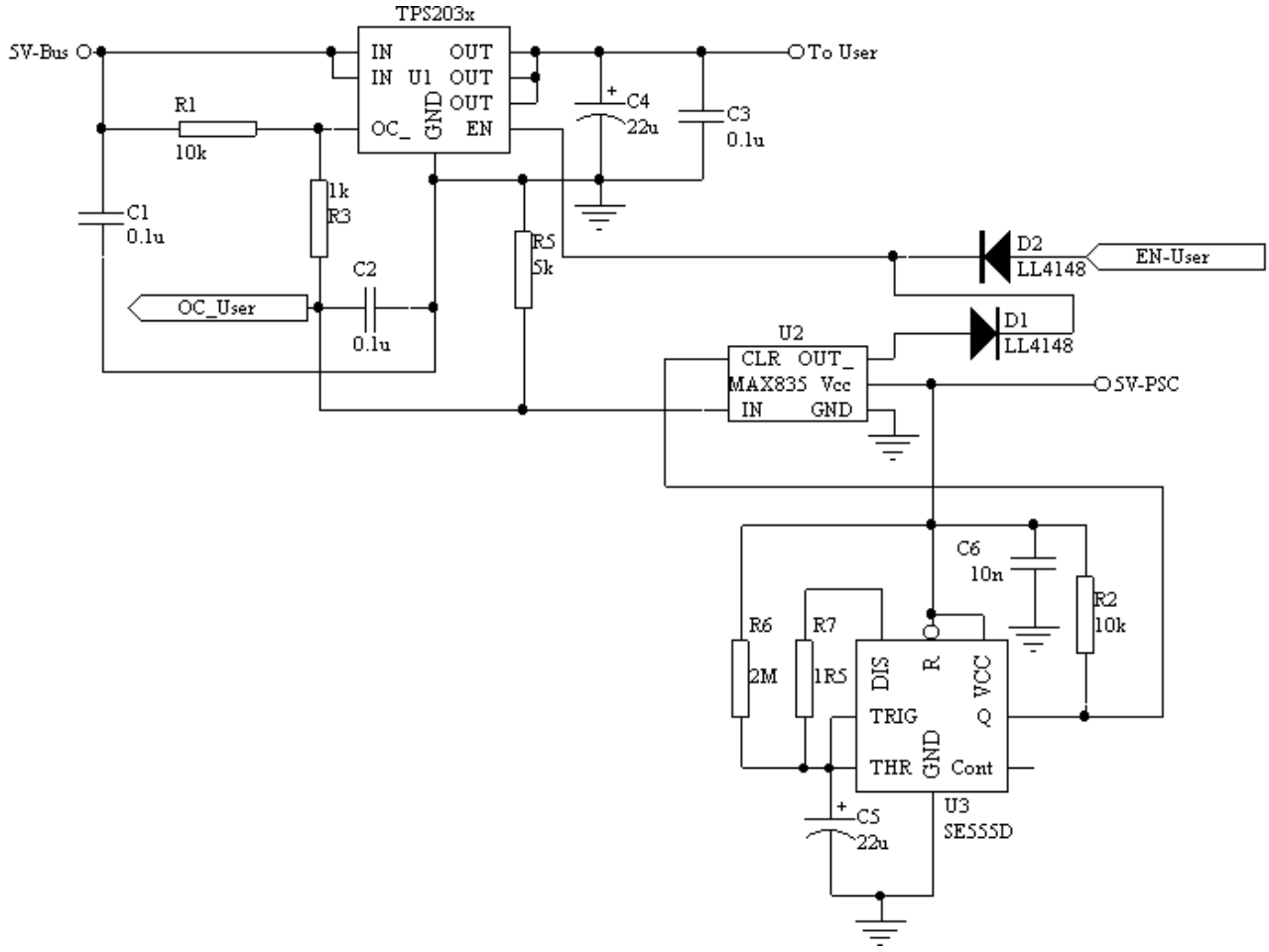


Figure 4.12 Protection circuits for each user

When the overcurent threshold is exceeded the power distribution switch TPS203x is limiting the output current and furnishing an overcurrent flag at $\overline{OC}$ output. This signal is filtered for avoiding false overcurrent signals which can occur because of the transients. The micropower voltage monitor MAX835 is comparing the filtered $\overline{OC}$ signal with its internal reference. If the signal is smaller than the reference the internal latch will put the output of the MAX835 low. The output is connected through a diode to EN pin of the TPS203x inhibiting in this way the output of the device. EN pin can be also inhibited by the MCU.

The latches are periodically cleared using an astabil. The circuit used is the precision timer SE555D configured in astable operation mode and the timing period is below one minute.

4.5.1. Power distribution switches TPS203x

The TPS203x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50mΩ N-channel MOSFET high-side power switches. The main characteristics of this family are:

- 33mΩ (5V Input) High-Side MOSFET Switch
- Short-Circuit and Thermal Protection
- Overcurrent Logic Output
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- Typical Rise Time . . . 6.1 ms
- Undervoltage Lockout
- Maximum Standby Supply Current ...10 mA
- No Drain-Source Back-Gate Diode
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

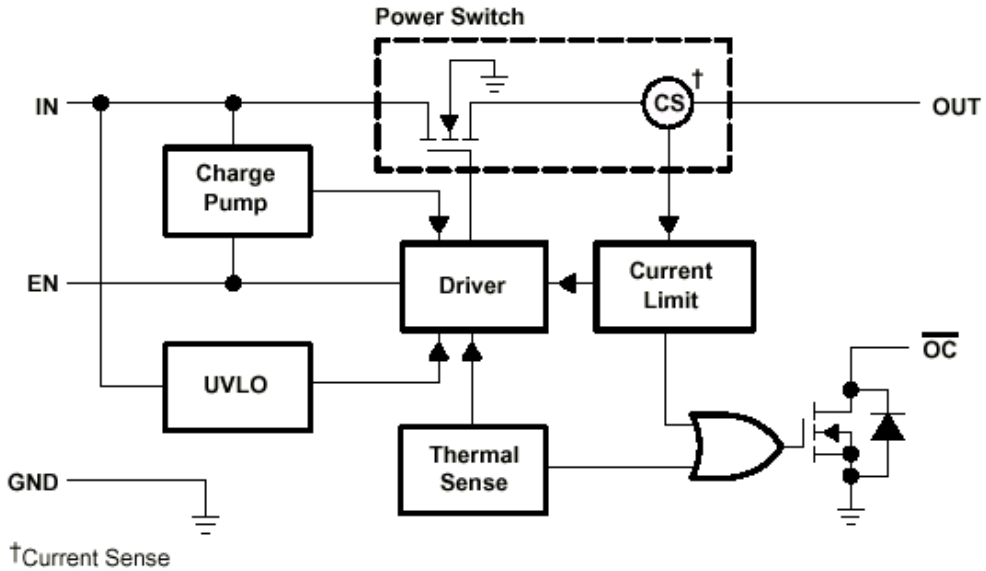


Figure 4.13 Functional diagram for power distribution switch TPS203x

Pin Description

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
4	EN	I	Enable input. Logic high turns on power switch.
1	GND	I	Ground
2, 3	IN	I	Input voltage
5	$\overline{OC}$	O	Overcurrent. Logic output active low
6, 7, 8	OUT	O	Power-switch output

Detailed description

- **power switch**

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50mΩ ($V_{I(IN)}$ = 5V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

- **charge pump**

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

- **driver**

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

- **enable (EN)**

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10mA when a logic low is present on EN . A logic high input on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

- **overcurrent ($\overline{OC}$)**

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

- **current sense**

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered,

the current-sense circuitry sends a control signal to the driver. The driver, in turn, reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

- **thermal sense**

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

- **undervoltage lockout**

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2V, a control signal turns off the power switch.

AVAILABLE OPTIONS

DEVICES	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT [A]	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C [A]
TPS2030D	0.2	0.3
TPS2031D	0.6	0.9
TPS2032D	1	1.5
TPS2033D	1.5	2.2
TPS2034D	2	3

Table 4.3 Available options for TPS203x ICs

Considering the table 4.3 and the consumption for each user, the following devices have been chosen, stated in table 4.4:

No.	Consumer	Power [W]	Current[A]	Device
1	OBC	0.46	0.092	TPS2030D
2	Transmitter	9	1.8	TPS2034D
3	Camera	0.3	0.06	TPS2030D
4	Attitude Control	0.25	0.05	TPS2030D

Table 4.4 Choose of the protections circuits for loads

Figure 4.14 shows the TPS203x typical application circuit.

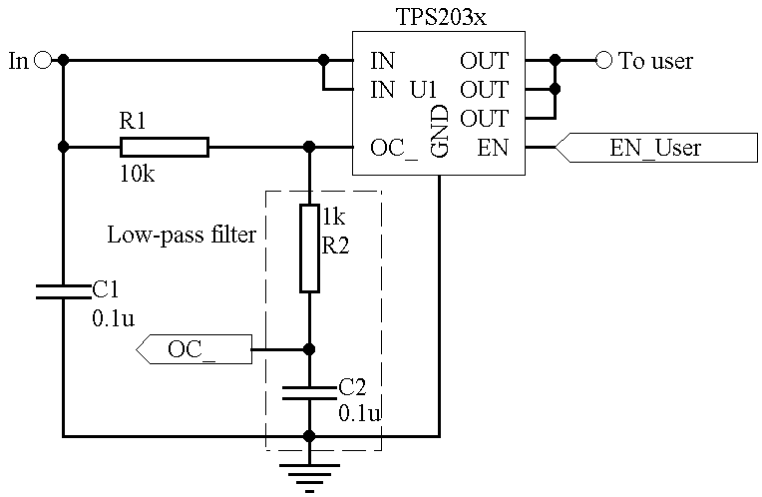


Figure 4.14 Application scheme for power distribution switch TPS203x

The filter at the $\overline{\text{OC}}$ output (R_2-C_2) is an low-pass filter and is reducing the false overcurrent reports. This can occur when heavy capacitive loads are connected and the inrush current is flowing through the device. The filter has a time constant of:

$$\tau = R_2 \cdot C_2 = 10^3 \cdot 10^{-7} = 100[\mu s] \tag{4.26}$$

and the turn-over frequency of

$$f_0 = \frac{1}{2 \cdot \pi \cdot \tau} = \frac{1}{2 \cdot 3.14 \cdot 10^{-4}} \approx 1591[\text{Hz}] \tag{4.27}$$

4.5.2. Micropower voltage monitor MAX835

The MAX835 micropower voltage monitor contains a 1.204V precision bandgap reference, comparator, and latched output in a 5-pin SOT23 package. The MAX835 has a push/pull output driver. Two external resistors set the trip-threshold voltage.

Applications

- Precision Battery Monitor
- Load Switching
- Battery-Powered Systems
- Threshold Detectors

Features

- Prevents Deep Discharge of Batteries
- Precision ±1.25% Voltage Threshold

- Latched Output (once low, stays low until cleared)
- SOT23-5 Package
- Low Cost
- Wide Operating Voltage Range, +2.5V to +11V
- <2µA Typical Supply Current
- Push/Pull Output

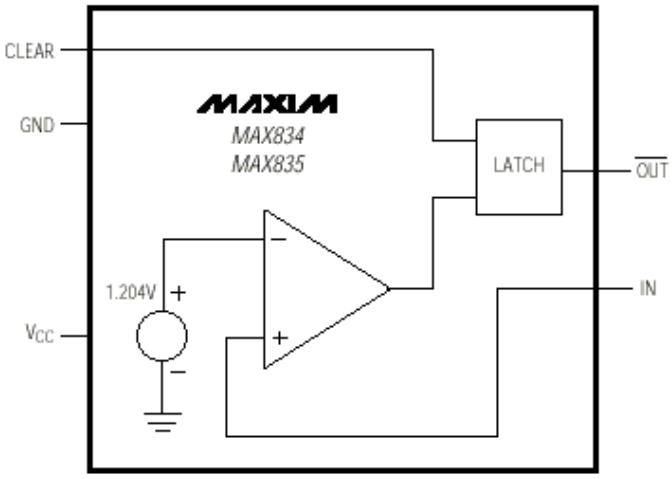


Figure 4.15 Functional diagram for MAX835 micropower voltage monitor

Programming the Trip Voltage (V_{TRIP})

Two external resistors set the trip voltage, V_{TRIP} (figure 4.16). V_{TRIP} is the point at which the falling monitored voltage causes OUT to go low. IN's high input impedance allows the use of large-value resistors without compromising trip voltage accuracy.

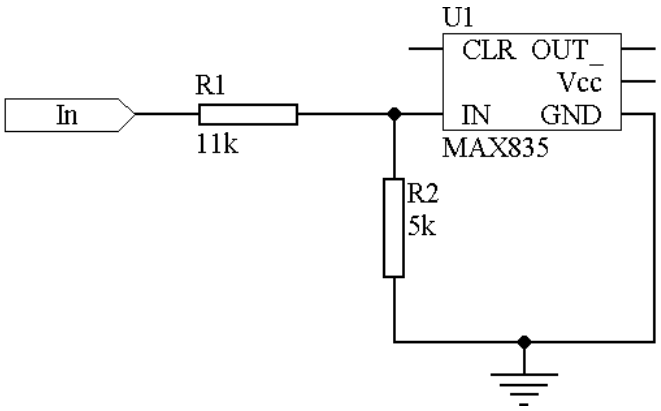


Figure 4.16 Setting the V_{TRIP} voltage

Knowing that the R_1 is form from two resistors in series (see in figure 4.12 the resistors R_1 and R_3) the resultant value for R_1 is 11kΩ. The value for R_2 is computed as it follows:

$$R_2 = \frac{R_1}{\left(\frac{V_{TRIP}}{V_{TH}} - 1\right)} \tag{4.28}$$

where V_{TRIP} is the desired trip voltage and V_{TH} is the threshold voltage and equals with 1.204V. This yields to:

$$R_2 = \frac{11 \cdot 10^3}{\left(\frac{4}{1.204} - 1\right)} = 4736.7\Omega \tag{4.29}$$

and the final value for the resistor of 5kΩ. The trip voltage was establish knowing that the input voltage should be smaller that the supplying voltage with 0.25V. Is not needed a too precise programming for the trip voltage. The most important thing is to make the difference between a high or low logical state input

Latched-Output Operation

When V_{MON} falls below V_{TRIP}, OUT goes low and remains low (even if V_{MON} rises above V_{TRIP}), until CLEAR is pulsed high again with $V_{MON}>V_{TRIP}$. Figure 4.17 shows the timing relationship between V_{MON}, OUT, and CLEAR.

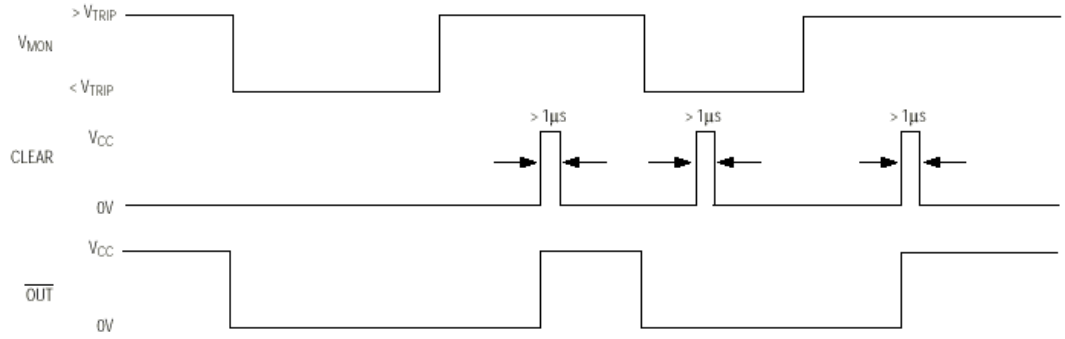


Figure 4.17 Relationship between V_{MON}, OUT, and CLEAR

4.5.3. Precision timer SE555D

Description

This device is precision monolithic timing circuit capable of producing accurate time delays or oscillations. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of VCC. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. RESET can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between DISCH and ground.

The output circuit is capable of sinking or sourcing current up to 200mA. Operation is specified for supplies of 5V to 15V. With a 5V supply, output levels are compatible with TTL inputs. The SE555 and SE555C are characterized for operation over the full military range of –55°C to 125°C.

Features

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source up to 200 mA

Functional diagram

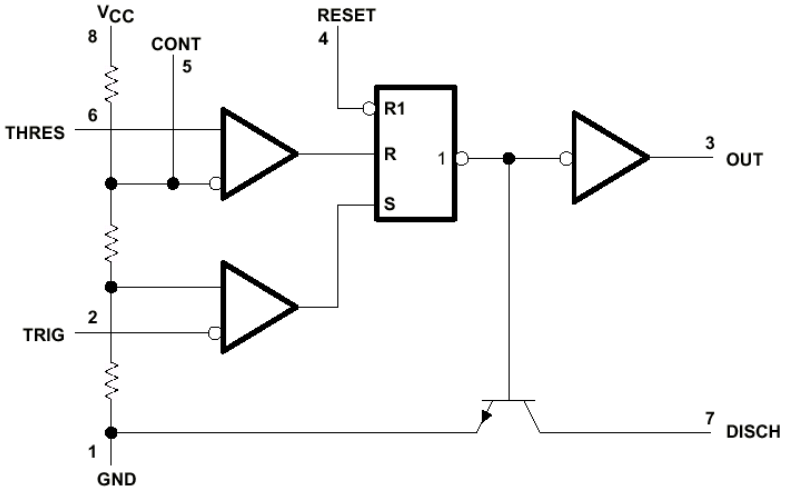


Figure 4.18 Functional diagram for SE555 IC

Application circuit

The application circuit diagram is shown in figure 4.19.

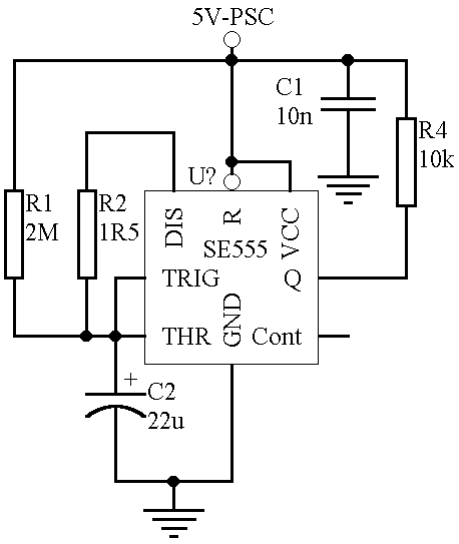


Figure 4.19 Application circuit for astable operation

Astable operation

As shown in figure 4.19, connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_1 and then discharges through R_2 only. Therefore, the duty cycle is controlled by the values of R_1 and R_2.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($0.67 \cdot V_{CC}$) and the trigger-voltage level ($0.33 \cdot V_{CC}$). The charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.

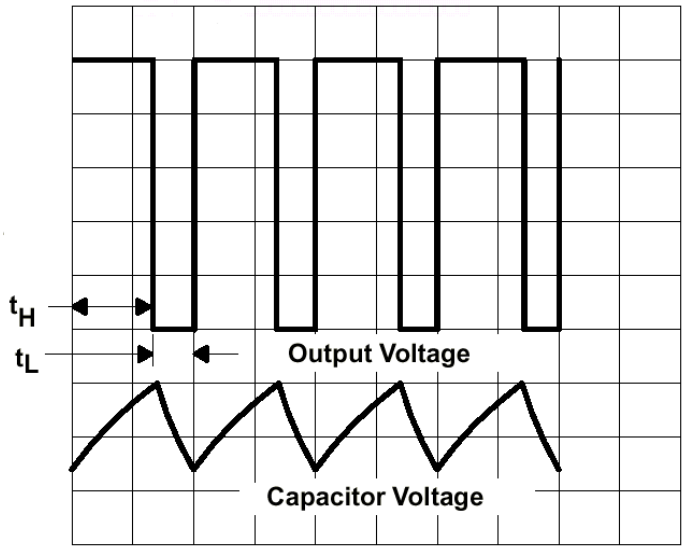


Figure 4.20 Typical astable waveforms

Figure 4.20 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693 \cdot R_1 \cdot C_2 \tag{4.30}$$

$$t_L = 0.693 \cdot R_2 \cdot C_2 \tag{4.31}$$

For clearing the MAX835 latch it is specified in the datasheet a minimum pulse width of 1μs. For ensuring the clear, it was selected the pulse width generated by SE555 (t_H) of 20μs. The time between the pulses (t_L) it was selected a value of 30s. It yields to:

$$t_H = 0.693 \cdot R_1 \cdot C_2 = 20[\mu s] \Rightarrow R_1 \cdot C_2 = 28.86 \cdot 10^{-6}[s] \tag{4.32}$$

$$t_L = 0.693 \cdot R_2 \cdot C_2 = 45[s] \Rightarrow R_2 \cdot C_2 = 43.29[s] \tag{4.33}$$

and considering the standardized values for components it was chosen: $R_1 = 1.5\Omega$, $R_2 = 2M\Omega$ and $C_2 = 22\mu F$. For these values of the components the new times are:

$$t_H = 0.693 \cdot 1.5 \cdot 22 \cdot 10^{-6} = 22.87[\mu s] \tag{4.34}$$

$$t_L = 0.693 \cdot 2 \cdot 10^{6} \cdot 22 \cdot 10^{-6} = 30.49[s] \tag{4.35}$$

4.6. Load filters

For a precise computing of the output filters for each load is necessary to know the value of the filtering capacitors placed on each board of the loads. Without this information is difficult to estimate the value of the filtering capacitors on the power supply board. A too high value for the capacities can generate huge inrush currents. A small one it cannot minimize enough the voltage ripple.

4.7. Housekeeping data acquisition

Housekeeping data are data collected in the satellite and delivered to the OBC to be sent down to the ground station. Values processed are currents, voltages and temperatures.

4.7.1. Measurement of currents and voltages

As described in section 3.4.3, the measured currents in the satellite are:

- currents on each solar panel

- current flowing from step-up converter
- currents flowing to each user

Similarly, the voltages collected are:

- voltage on the solar panels, at the input of the step-up converter
- voltage of the batteries
- voltage on the regulated bus

Measurement of the currents

The current is measured using shunt resistors. The voltage drop on the shunt resistors is proportional with the current flowing through the resistor. From the specifications is known that the voltage for each user should be within 2% accuracy. This means a voltage of 100mV. For this reason the voltage drop on the shunt resistors should smaller than this value. Because the A/D converter has a 12bit resolution (approx. 1.22mV voltage step), for a voltage range lower than 100mV the error will be quite big when small currents are measured.

Taking in consideration this it seems that the small voltage drop on the shunt must be amplified to 5V, the maximum input voltage for A/D converter of the microcontroller. For this reason is used the high-side current-sense amplifier MAX4372. Because the input voltage is very low, it can be easily affected by parasites, a low-pass filter is needed at the input. The measuring scheme can be seen in the figure 4.?.

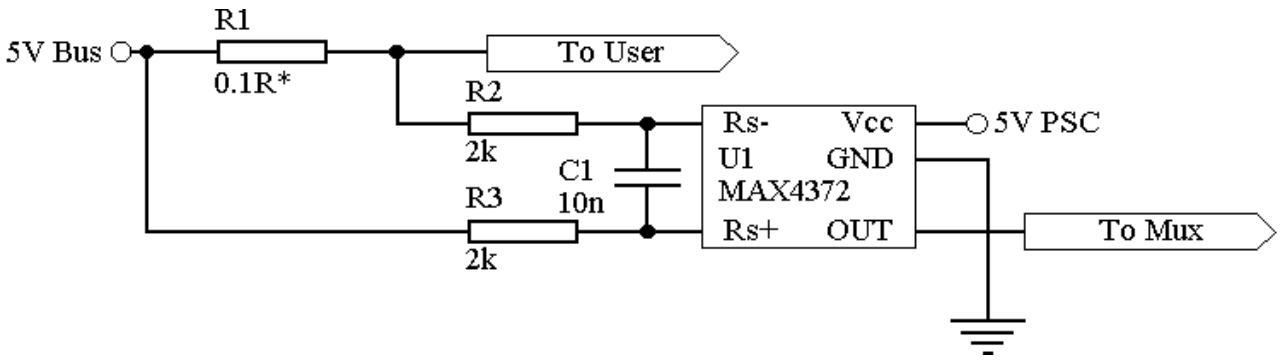


Figure 4.21 Current measuring circuitry

The differences between the measuring circuits for the current is the value for the resistor R_1 and the terminations of the MAX4372 IC's, which is indicating the voltage gain.

High-side current-sense amplifier MAX4372

The MAX4372 low-cost, precision, high-side current-sense amplifier is available in a tiny, space-saving SOT23-5 package. Offered in three gain versions (T = +20V/V, F = +50V/V, and H = +100V/V), this device operates from a single +2.7V to +28V supply and consumes only 30µA. It

features a voltage output that eliminates the need for gain-setting resistors and is ideal for today's notebook computers, cell phones, and other systems where battery/DC current monitoring is critical. High-side current monitoring is especially useful in battery-powered systems since it does not interfere with the ground path of the battery charger. The full-scale current reading can be set by choosing the device (T, F, or H) with the desired voltage gain and selecting the appropriate external sense resistor. This capability offers a high level of integration and flexibility, resulting in a simple and compact current-sense solution.

Functional diagram

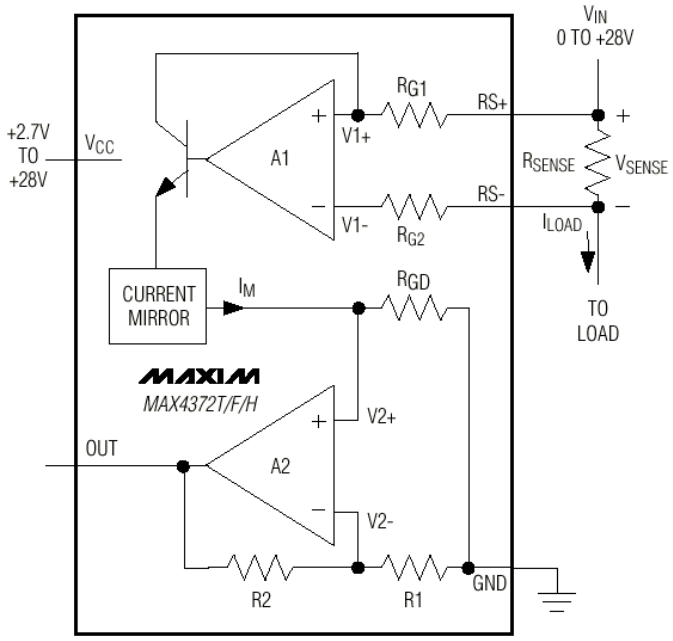


Figure4.22 Functional diagram for MAX4372

Features

- Low-cost, compact current-sense solution
- 30μA supply current
- +2.7V to +28V operating supply
- 0.18% full-scale accuracy
- Low 1.5Ω output impedance
- Three gain versions available:
  - +20V/V (MAX4372T)
  - +50V/V (MAX4372F)
  - +100V/V (MAX4372H)
- Wide 0 to +28V common-mode range, independent of supply voltage
- Available in space-saving SOT23-5 package

Pin description

Pin	Name	Function
1	GND	Ground
2	OUT	Output Voltage. V_{OUT} is proportional to the magnitude of V_{SENSE} (V_{RS+}-V_{RS-}).
3	V_{CC}	Supply Voltage
4	RS+	Power Connection to the External Sense Resistor
5	RS-	Load-Side Connection to the External Sense Resistor

Choosing R_{SENSE} (R_1)

Given the gain and maximum load current, R_{SENSE} will be selected such that V_{CC}-V_{OUT} does not exceed +0.25V. To measure lower currents more accurately, a high value for should be used for R_{SENSE}. A higher value develops a higher sense voltage, which overcomes offset voltage errors of the internal current amplifier. For monitoring high current, R_{SENSE} must be able to dissipate its own I^2R losses. If the resistor's rated power dissipation is exceeded, its value may drift or it may fail altogether, causing a differential voltage across the terminals in excess of the absolute maximum ratings.

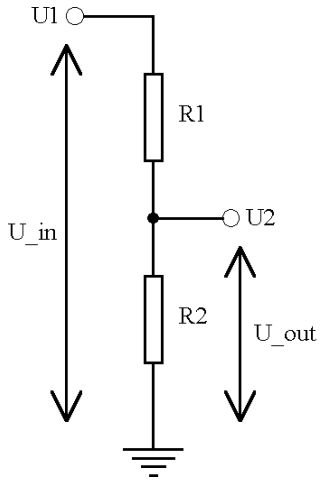
Following the considerations above, the fact that the voltage drop on the shunt should be lower than 100mV and the voltage scale limit of 4.5V the recommended component values from datasheet and the available values for the shunt resistors it yields:

No.	Consumer	Current [A]	Maximum current [A]	Shunt resistor [Ω]	Gain [V/V]	Device	Full-scale output voltage [V]
1	Solar arrays	0.462	0.5	0.1	50	MAX4372F	2.5
2	Battery	0.5A	0.5	0.25	20	MAX4372T	2.5
3	OBC	0.092	0.3	0.1	100	MAX4372H	3
4	Transmitter	1.8	3	0.01	100	MAX4372H	3
5	Camera	0.06	0.3	0.1	100	MAX4372H	3
6	Attitude Control	0.05	0.3	0.1	100	MAX4372H	3

Table 4.5 Choose of components for currents measurements

Measurement of the voltages

The voltages measured are above the maximum input voltage for the multiplexer so, voltage dividers will be used at the input of the multiplexer. All the voltages will be processed by MCU after the conversion in digital.



No.	Signal	Input voltage [V]	Output voltage [V]	R_1 [kΩ]	R_2 [kΩ]
1	Voltage on the solar panels	4.932	2.466	100	100
2	Voltage of the batteries	6-8.4	4.2	100	100
3	Voltage on the regulated bus	5	2.5	100	100

Figure 4.23 Values for resistors used in voltage measurement

For reducing power consumption have been selected big values for the resistances.

4.7.1. Measurement of temperatures

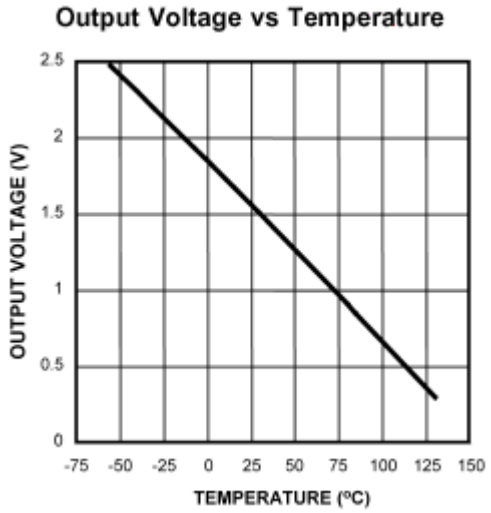
For housekeeping data and also for avoiding the critical state are useful values of temperatures inside the satellite. A system of 7 sensors will be distributed all over the satellite to measure temperatures on the most sensitive parts. This measure points will be selected in a virtue of thermal analysis. Results from these sensors can be used in thermal control.

The devices selected for temperature measurement must be as small as possible and must be able to operate in range of industrial standard (-55 to 85˚C). Communication with PIC controller must be also very simple, regarding to the number of wires used for communication with microcontroller. According to the specifications analog sensors are preferred, they need less wires for communication with multiplexer. Only voltage level will be sent to the multiplexer and then analog to digital converter, which is implemented in PIC controller will convert the value. For sticking device, epoxide or some special glue can be used. This system will be easy to implement and will be also very robust. The LM19 from National Semiconductors have been chosen to fulfill these specifications. The LM19 is a precision analog output CMOS integrated-circuit temperature sensor that operates over a -55°C to +130°C temperature range. Here are a few features and specifications. The attached CD contains datasheet for this sensor, also.

- rated for full -55°C to +130°C range
- available in a TO-92 package
- accuracy at +30°C ±2.5 °C (max)
- accuracy at +130°C & -55°C ±3.5 to ±3.8 °C (max)

- power supply voltage range +2.4V to +5.5V
- current drain 10 μA (max)
- nonlinearity ±0.4 % (typ)
- predictable curvature error

The accuracy of the LM19 when specified to a parabolic transfer function is ±2.5°C at an ambient temperature of +30°C. The temperature error increases linearly and reaches a maximum of ±3.8°C at the temperature range extremes. The temperature range is affected by the power supply voltage. At a power supply voltage of 2.7 V to 5.5 V the temperature range extremes are +130°C and -55°C. Decreasing the power supply voltage to 2.4 V changes the negative extreme to -30°C, while the positive remains at +130°C.



Temperature (°C)	Typical V_O (mV)
+130	+303
+100	+675
+80	+919
+30	+1515
+25	+1574
0	+1863.9
-30	+2205
-40°	+2318
-55	+2485

Figure 4.24 Output voltage vs. temperature and typical values for LM19

Shutdown capability for the LM19 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates or does not necessitate shutdown at all.

In figure 4.25 is depicted the implementation of temperature measurement. Power bus gives required voltage and the V_o is analog voltage output. For details see datasheet for LM19, on the attached CD of the report.

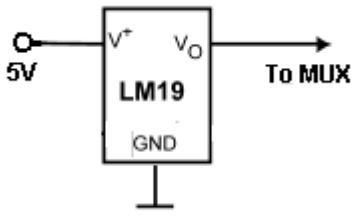


Figure 4.25 Temperature measurement circuitry

4.8. MCU – hardware and software

4.8.1. Selection of hardware

In the interface specification made by Cubesat steering committee [*interfaceV14.pdf*] are defined main parameters for hardware parts of MCU circuit and they must be fulfill. However, these parameters are only general and there is still lot of considerations to be done.

Microcontroller (MCU) must redeem these properties: it must have at least 12-bits analog-digital converter, supports I^2C bus in slave mode with 100kHz speed and it must acquire housekeeping data from the satellite. There are 14 electrical signals plus 7 temperatures to be measured.

From the demands can be evaluated minimum number of pins on the MCU. List of needed pins is on table 4.6. Number of pins for housekeeping data is calculated as a sum of needed analog input pins and digital control signals for multiplexers.

Name of the pin	**Number of pins**
Housekeeping data acqusition	7 pins
Boot pin	1 pin
Oscillator	2 pins
Power source	1 pin
Ground	1 pin
Fault signal from users	4 pins
Enable/Disable signal for users	4 pins
I^2C bus	2 pins
TOTAL	**21 pins**

Table 4.6 Description of needed pins

Another problem is program memory in the processor. Today's hi-tech FLASH technology could be used for space applications, but the probability that some high-energy particle from space will change memory is rising, to prevent this risk was decided to use OTP memories. For development is not good to have processor with no way how to erase it and reprogram again, so the chip that has been looking for was one with packages with erasable window (for debugging) and with OTP memory (for final product).

1. MCU

At the beginning was figured that 8-bit microcontroller is powerful enough for this task and there is no need to use processors that are more advanced. There is wide variety of types and families of 8-bit processors like AVR from Atmel, PIC from Microchip, Motorola 6800 family or

Intel 8051 family. Consumption of most of them is very high (for example 8051's consumption with 5V and 1MHz inner frequency is app. 100mW [*ADuC812_b.pdf*]), and low consumption is a priority number one for systems with limited electrical energy like Cubesat satellite. Also processors with reduced instruction set (RISC) have, because of their simplified inner structure very low consumption compare to the ones with wide instruction set. After these considerations was decided to search closely RISC microcontrollers.

After brief search of possible companies and also after consultations with other Cubesat's groups was decided to select one processor from Microchip, because ACS and COM modules will use this family so it is good idea to select same one for better compatibility and sharing development resources.

Last step was to decide which variant select. Removing chips without I^2C or without appropriate A/D converter or without enough pins only few possible solutions stayed. From them was selected PIC16C774, because it has parameters very corresponding with requested characteristics.

PIC16c774 is 8bit processor with reduced instruction set (RISC) manufactured in 40 and 44 pin packages. It has 10 possible inputs to the analog to digital converter with maximum speed of conversion 2μs.

It has two types of memory, for program it has 4kB OTP memory or 4kB EPROM memory (depending on package) and for data there is 256 bytes of RAM.

Processor has five input/output ports, where ports B, C and D are 8-bit ports, port A is 6-bit and port E is 3-bit. Not all ports can be used as a digital pins, because lot of functions are multiplexed with them (for example port A and E are multiplexed with A/D converter).

Among other features belongs PWM output, internal watchdog or low voltage detector. For more detail description, see datasheet [*30275a datasheet.pdf*].

2. Multiplexers

Multiplexer is simply described, digitally controlled switch among some inputs to the one output and the main purpose in the PSU is to collect more signals than there are free pins on the MCU. There are more possibilities which multiplexers use in PSU, as was written in specifications and analysis PSU will send 21 signals to OBC. In that case, two 16 to 1 channels multiplexers can be used or three 8 to 1 channels multiplexers are also possible. 8-1 muxes have less control wires, they need only three compare to four for 16-1 muxes, but they need one more analog input and more space on PCB, actually they are smaller but with all power supply wires and control signals result will be the same as with 16-1muxes. Finally two 16-1 multiplexers were chosen. Another

advantage of them is that at this moment, only 21 signals are measured, but if in the future anyone will want to add signal, there will be no problem with it at all. As a conclusion were selected multiplexers from Analog Devices ADG706, which have very small R_{on} resistance 2.5Ω [*ADG706_7_0.pdf*], and they have acceptable size (10mmx6.5mm).

3. Switching between MPPT signals

Because there will be three types of driving signals for MPPT converter, there must be switch among them. From this is clear that some sort of arbitrate system is needed. Digital controlled switch consists only from one 4 to 1 channel multiplexer, 3 to 1 multiplexer should be sufficient for it, but they are not common on the market. Deeper look inside the problematic is done in another chapter. Final decision was made to use another multiplexer from Analog Devices (ADG704), because of their low R_{on} resistance [*ADG704_a.pdf*].

4. Oscillator

The oscillator is one of the most important parts in MCU circuits and there are more ways how to guarantee frequency for MCU: Resonant crystal, resonant oscillator or resonant *RC* circuit. First two variants are very precious, but they are sensitive to mechanical ripples and their maximum mechanical stress is 10G [*7702.pdf*] what is starting to be close to the launching start stress (7G) [*Hansen, 2001*]. After comparing these facts was decided to use resonant *RC* circuit, which is not too precise and is vulnerable to temperature, but for tasks, which MCU is going to be used, precise timing is not needed. Does not matter if frequency is 3MHz or 5MHz. This oscillator consists only of two components and these components are simple resistor and capacitor, reliability of this circuit is much higher compare to resonant crystal. On figure 4.1 is shown connection of RC circuit to MCU.

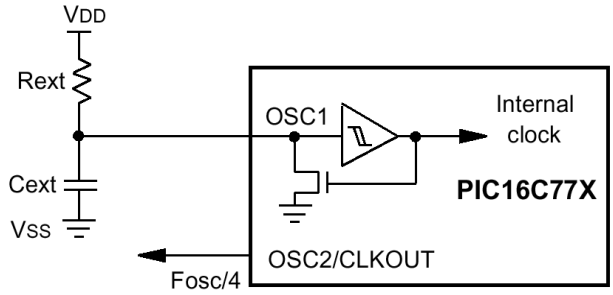


Figure 4.26 Scheme of RC oscillator

Following the recommendations from manufacturer [*Mid-Range MCU Family Reference Manual, p. 2-12*], where they recommended resistance between 3k and 100kΩ and capacitance

above 20pF. Values for R_{EXT} and C_{EXT} have been selected R_{EXT} = 4.7kΩ and C_{EXT} = 22pF (experimental approach to obtain 4MHz frequency).

4.8.2. Hardware design

1. Connection of protection circuits

Protection circuits need eight digital signals for their right function. Four of them are inputs and the rest are outputs, each user has it's own pair of these signals. Input signals are called NOT_FAULT signals, because when this signal is in high state, the user works fine. When the low state is set means that protection circuit detected overcurrent. Second signal is ENABLE and provide turn on/off signal for protections. When ENABLE is in the high state user is turn on.

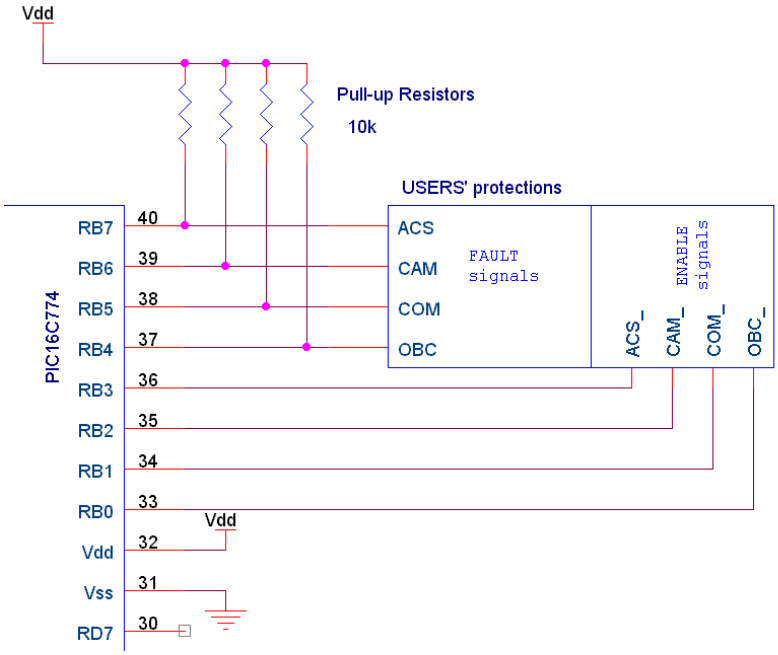


Figure 4.27 Connection of protections

Because protection circuits work as a current limiter, MCU do not need to provide turn-off of the users too quickly, but still it is better to turn off user at least in few ms. PIC16C774 has good technical solution for this problem; it is called "interrupt on change on port B". Simply explained: MCU run interrupt routine when change from low to high state (or high to low state) on port B (bits 4,5,6 and 7) occurs. When using interrupts, user could be turn off in few moments. Usually for input pins are needed pull-up resistors, otherwise signal should not has perfect high state (low level is done by connecting to the ground and high level is done by not connecting anywhere and wire is "in the air"). Solution for this these pull-up resistors, there is already weak pull-up resistors inside the MCU, but they can be used only when they are set by software. To be sure that signal will correct

value was decided to use external ones too, these external pull-up resistors are already part of protection design so no more component will be added (see section 4.5).

Enable signals may be connected to any output pin on MCU, but to have all things around protections on one place, it is good to use rest of pins from port B for ENABLE.

2. Signals connection

All signals collected from PSU are connected to the MCU through the multiplexers, but because not all signals have same priority or voltage levels, some design changes must be implemented.

There are two main groups of signals: electrical and thermal. Because temperature cannot change too fast, it is not needed to read thermal sensors so often as electrical signals. All electrical signals should be put together to one multiplexer and thermal sensors to another one. The second multiplexer will be read only every few seconds. More details about this can be found in section 4.8.3.

Because analog/digital converter can convert voltages in resolution V_{ref-} to V_{ref+} (in this case from 0 to 5V), signal connected to the ADC cannot be higher or lower than these values. To decrease the voltage level a voltage divider is used, rate ½ is used for better digital processing (multiplication by two is done just by adding same value). It means all three measured voltages (solar panels, batteries and 5V bus) will be twice smaller. Rest of the signals (currents) can be measured directly.

For thermal sensors used in the satellite (LM19), which have maximum voltage around 3V, no voltage divider is needed and mux2 can be directly connected to the ADC. The scheme of implementation for the MCU is shown in Appendix C.

Each multiplexer must be driven by four control signals. Because there is no need to read both multiplexers at the same time, these four signals from each multiplexer can be connected together and only four wires connected to any four output pins on the MCU.

3. Power source connection

Separate analog and digital power supply pins (V_{dd} and AV_{dd}, respectively) allow AV_{dd} to be kept relatively free of noisy digital signals often present on the system V_{dd} line. Connection scheme is presented in figure 4.28. Smaller capacitors (0.1μF) must be connected as close to the power pins as possible to keep trace lengths short.

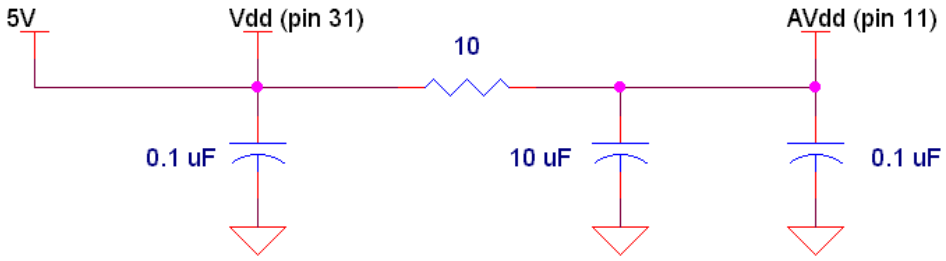


Figure 4.28 Power source connection

4. Digital MPPT circuits

For digital version of MPPT controller is needed an analog output in range from 0 to 1.5V. Unfortunately, the PIC16C774 does not have any D/A converter included. This problem can be override with MCU's PWM output and all what is needed is a low-pass filter to create an analog signal. Because MCU will run on low frequency to lower power consumption, PWM cannot run too fast without loss of resolution. Resolution was selected 9 bits when voltage step should be:

$$MaxStep = \frac{V_{REF}}{2^{rezolution}} = \frac{5(V)}{2^9} = 10(mV) \tag{4.36}$$

and the frequency can be up to 7.4kHz.

The output signal of the filter will be MPPT control signal and this signal is changing only in dependence on rotating of the satellite or when temperature change. These changes are relatively slow and bandwidth of this signal should be very low, only few hertz (it was established 100 Hz). That is the reason why 7.4KHz will be enough for PWM frequency. Values for the filter were counted from the following relation:

$$R \cdot C = \frac{1}{2 \cdot \pi \cdot f} \tag{4.37}$$

and if C is chosen as 330nF , a resistance R = 4.8kΩ is the result.

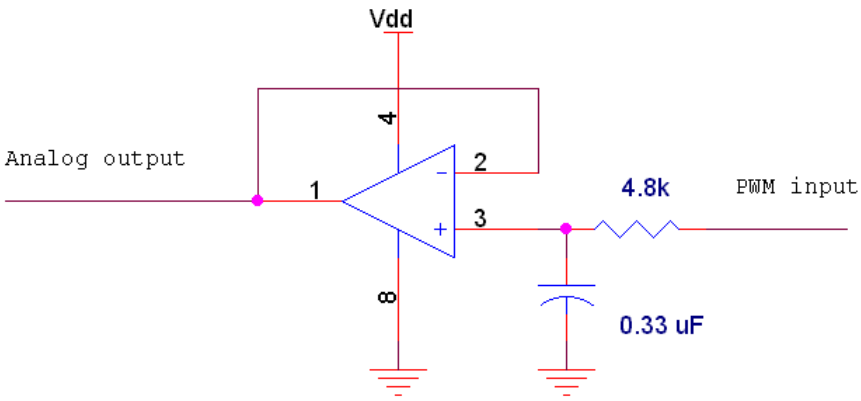


Figure 4.29 Low pass filter for PWM signal

5. System for arbitrating MPPT signals

As a system for selecting which system will drive MPPT converter was selected 4->1 multiplexer, controlled by MCU. This MCU will watch the analog signal and after it will stop work, MCU switch to another source (digital or default), when MCU hang or crash and will be unable to control multiplexer, watchdog will reset MCU and default values will be set on the pins (logic 0) and this default values on the multiplexer will select default MPPT signal (see the truth table on table 4.7).

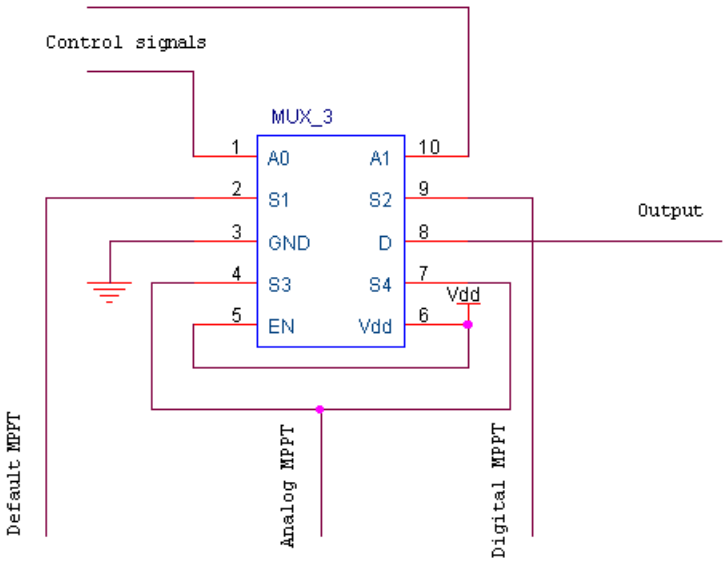


Figure 4.30 Arbitrating system

Output	A0	A1	EN	MPPT
S1	0	0	1	Default
S2	1	0	1	Digital
S3	0	1	1	Analog
S4	1	1	1	Analog
N/A	X	X	0	N/A

Table 4.7 Truth table for MUX3

4.8.3. Software for MCU

1. Basic structure

There are two main parts of the software. The first one, which is time crucial, was created as interrupt service routines. Time is important for serial communication and for protections. For the rest is not needed that fast response and they could be done as a normal code in main loop.

On figure 4.31 is displayed the structure of both parts.

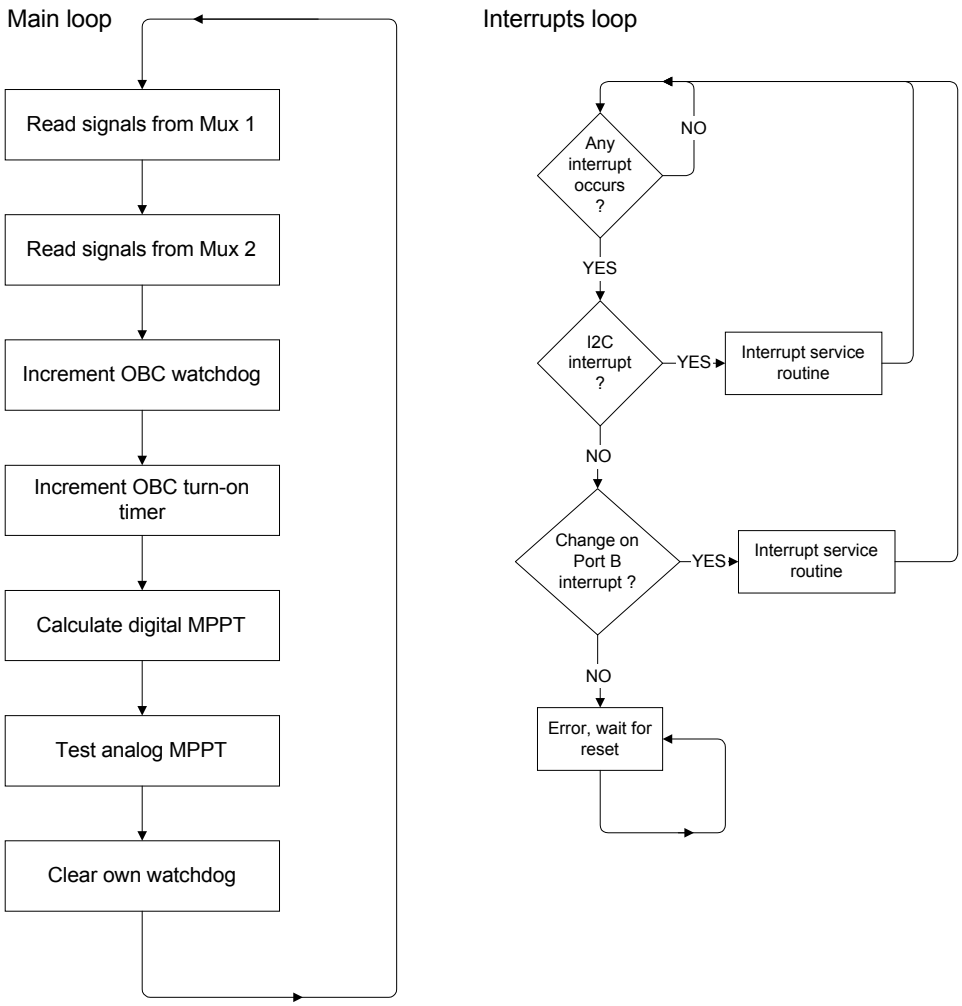


Figure 4.31 Program structure

2. Protections

Protections are systems, which need relatively fast response. It was decided to use interrupt routines to service them. After any change occurs on the pins configured as the inputs for NOT_FAULT signals, software will detect which users has overcurrent and turn off that user. The flowchart, describing algorithm, is depicted in figure 4.32a.

3. Data acquisition

Converting signal from analog voltage to digital number is very important task for MCU, because most of the functions of the MCU depending on these signals. An error in data acquisition will cause another errors in other parts of software. PIC16C774 has implemented 12bit A/D converter, which implies that for each sensor is needed two bytes of memory (not all bits will be used in these two bytes). These two bytes will be overwritten every time ADC converts updated value. No past values are stored, for calculating average, maximum or minimum values special software should be in the OBC. The algorithm of reading signals is explained on figure 4.32b.

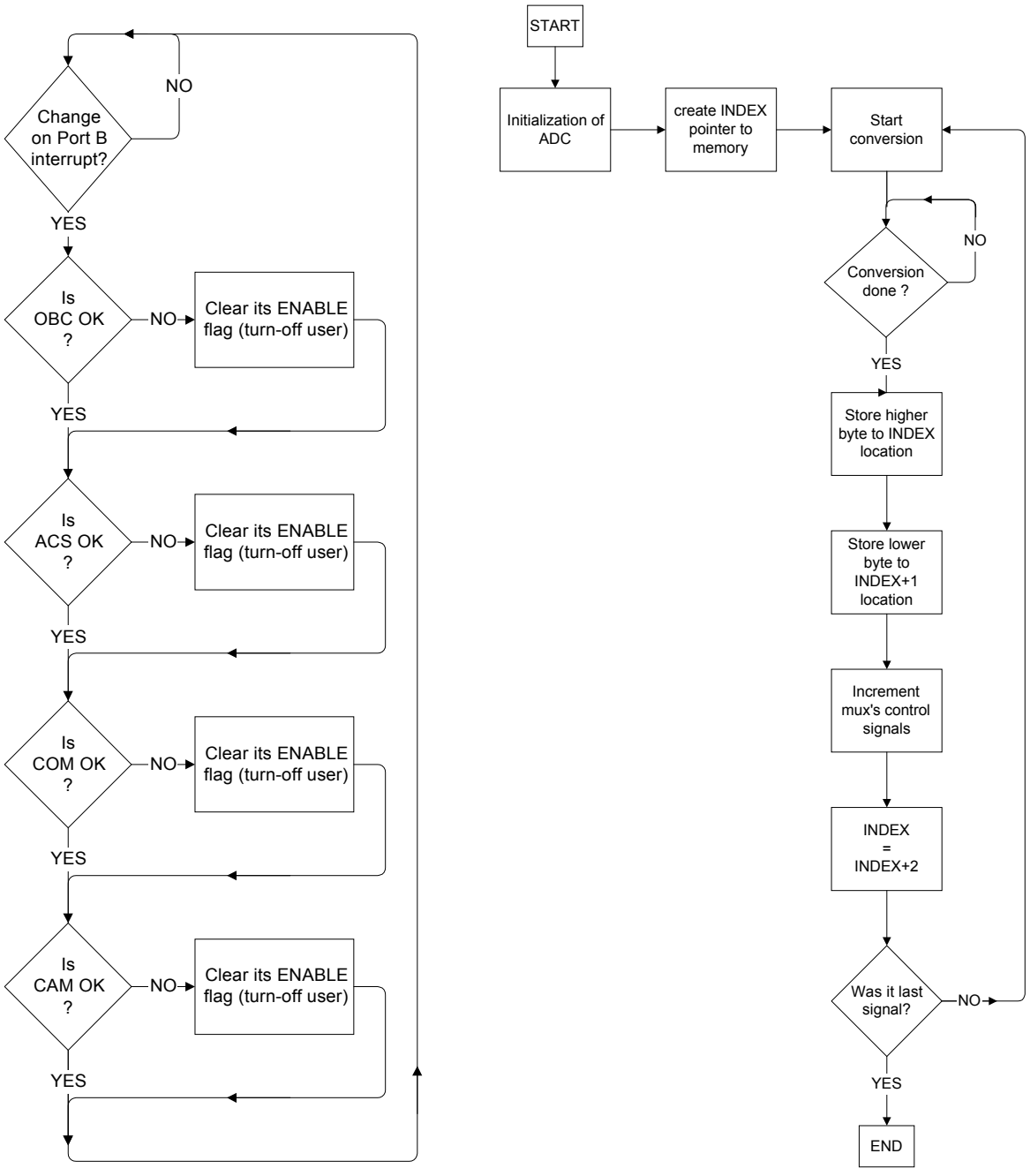


Figure 4.32 Protections' interrupt service routine (a) and algorithm for reading signals from mux1(b)

Figure 4.32b is only for one multiplexer, but both multiplexers have same function, only memory places and input pins are changing. Another difference is that values from mux2 are voltages from temperature sensors and these voltages will be converted to the degrees of Celsius. Because accuracy of the sensor is app. ± 3°C there is no need for 12-bit number and was decided to use 8-bit for better manipulation. Further was decided to use binary complement format for numbers (-1 is FFh, 0 is 0h and 1 is 1h and so on, numbers can be from –127 to 128). The fastest

way how to convert numbers is to use look-up table with pre-calculated values from approximation equation for sensor [*LM19.pdf*].

$$T = \frac{1.8528 - V}{0.01179} \tag{4.38}$$

where T is the temperature [°C] and V is measured voltage [V].

4. I²C bus communication

I²C is two wires bi-directional bus; PSU will work as a slave on this bus. [*I2C-busv1_7.pdf*]. Each byte, which should be sent to PSU from OBC, is stored in SSPBUF and then interrupt is created. After MCU read that byte, OBC can continue with sending another byte. Similar is it with writing to bus; only interrupt is created each time when OBC read successfully byte, which MCU send through SSPBUF to the bus.

Data buffer

Because housekeeping data should be collected also during sending them to OBC, I²C cannot send data directly from places in the memory where ADC saved them, because they can be changed there during transmition. It was decided to use another place in the memory to store whole module in some sort of buffer, its structure is on figure 4.33. When OBC request first byte from new module, MCU first fill this buffer with values from ADC and compute CRC and header. After OBC request another bytes, only index pointer will be incremented and prepared byte will be sent.

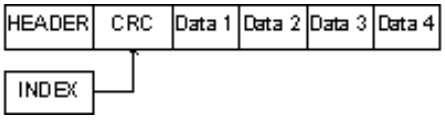


Figure 4.33 Structure of the buffer

States of the I²C bus

There are five possible states on I²C bus:

- State 1, Master will send data to slave and byte, which is in the SSPBUF is the address of the PSU and nothing will be done with this byte
- State 2, Master sends data to slave and byte, which is in the SSPBUF, is data package and must be read and processed.
- State 3, Slave will send data to the OBC and in SSPBUF is PSU address. Buffer must be filled and CRC calculated. Then HEADER will be written to the SSPBUF as a first byte of the module.

- State 4, Slave sends data to the OBC and module sending is in progress, byte where INDEX pointing will be written to the SSPBUF and after INDEX will be incremented.
- State 5, Master resets I2C logic, all buffer and INDEX pointer will be cleared.

Description of modules

For communication with OBC were created two types of modules, one for each direction of communication. Each module includes header and CRC and could include four bytes of data. Inner structure of the header is on figure 4.34. CRC is calculated as a sum of all bytes in module (header + data). For more detailed information about header and CRC see [*I2C-busv1_7.pdf*].

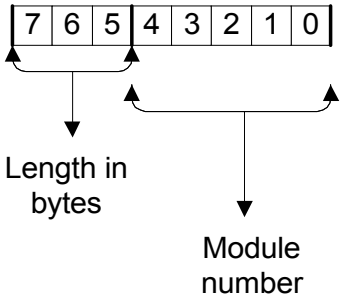


Figure 4.34 Structure of the header byte

Module nr.	1st byte	2nd byte	3rd byte	4th byte
1	Battery voltage (Higher byte)	Battery voltage (Lower byte)	Current from MPPT (Higher byte)	Current from MPPT (Lower byte)
2	SC 1 current (Higher byte)	SC 1 current (Lower byte)	SC 2 current (Higher byte)	SC 2 current (Lower byte)
3	SC 3 current (Higher byte)	SC 3 current (Lower byte)	SC 4 current (Higher byte)	SC 4 current (Lower byte)
4	SC 5 current (Higher byte)	SC 5 current (Lower byte)	SC voltage (Higher byte)	SC voltage (Lower byte)
5	5Volts bus voltage (Higher byte)	5Volts bus voltage (Lower byte)	PSU current (Higher byte)	PSU current (Lower byte)
6	Temperature 1	Temperature 2	Temperature 3	Temperature 4
7	Temperature 5	Temperature 6	Temperature 7	Protection status flag
8	OBC current (Higher byte)	OBC current (Lower byte)	CAM current (Higher byte)	CAM current (Lower byte)
9	COM current (Higher byte)	COM current (Lower byte)	ACS current (Higher byte)	ACS current (Lower byte)
19	This module has no data inside, this module will be send as a error message after wrong recalculation of CRC of message from OBC.			
20	This module has no data inside this module will be send as a OK message after successful recalculation of CRC from OBC			

Table 4.8 Modules from PSU, for OBC

Modules for communication from PSU to OBC are described in table 4.8. Modules for the other direction do not have any data inside; they consist only from header and CRC, which must be same as header. Modules from OBC are described in table 4.9.

Module nr.	Description	Module nr.	Description
1	Request for module nr.1, PSU will send module nr.1 next time.	22	Turn off ACS command
2	Request for module nr.2	23	Turn off CAM command
3	Request for module nr.3	24	Turn off COM command
4	Request for module nr.4	25	Turn on OBC command
5	Request for module nr.5	26	Turn on ACS command
6	Request for module nr.6	27	Turn on CAM command
7	Request for module nr.7	28	Turn on COM command
8	Request for module nr.8	29	Reset watchdog
9	Request for module nr.9	30	Clear bootpin (OTP PROM)
21	Turn off OBC command	31	Set bootpin (EEPROM/FLASH)

Tab 4.9 Modules from OBC, for PSU

I²C data flow algorithms

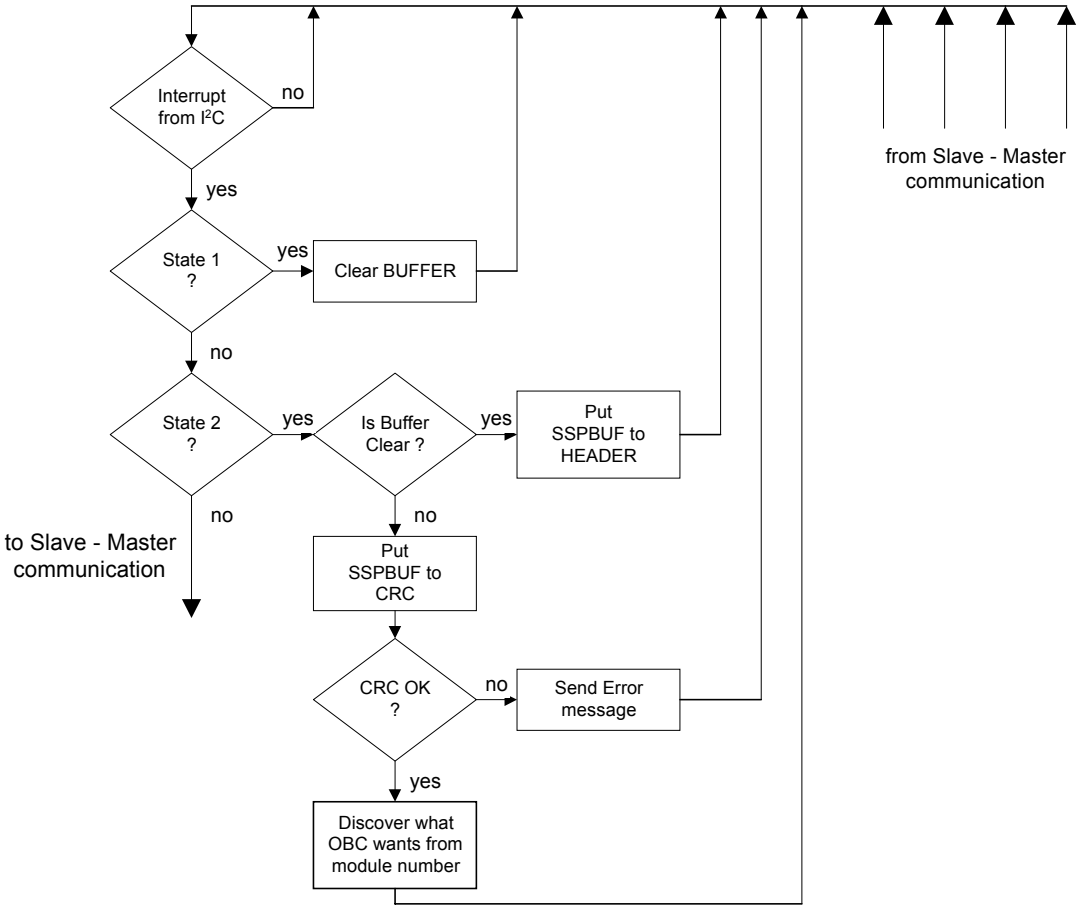


Figure 4.35 Communication from master to slave

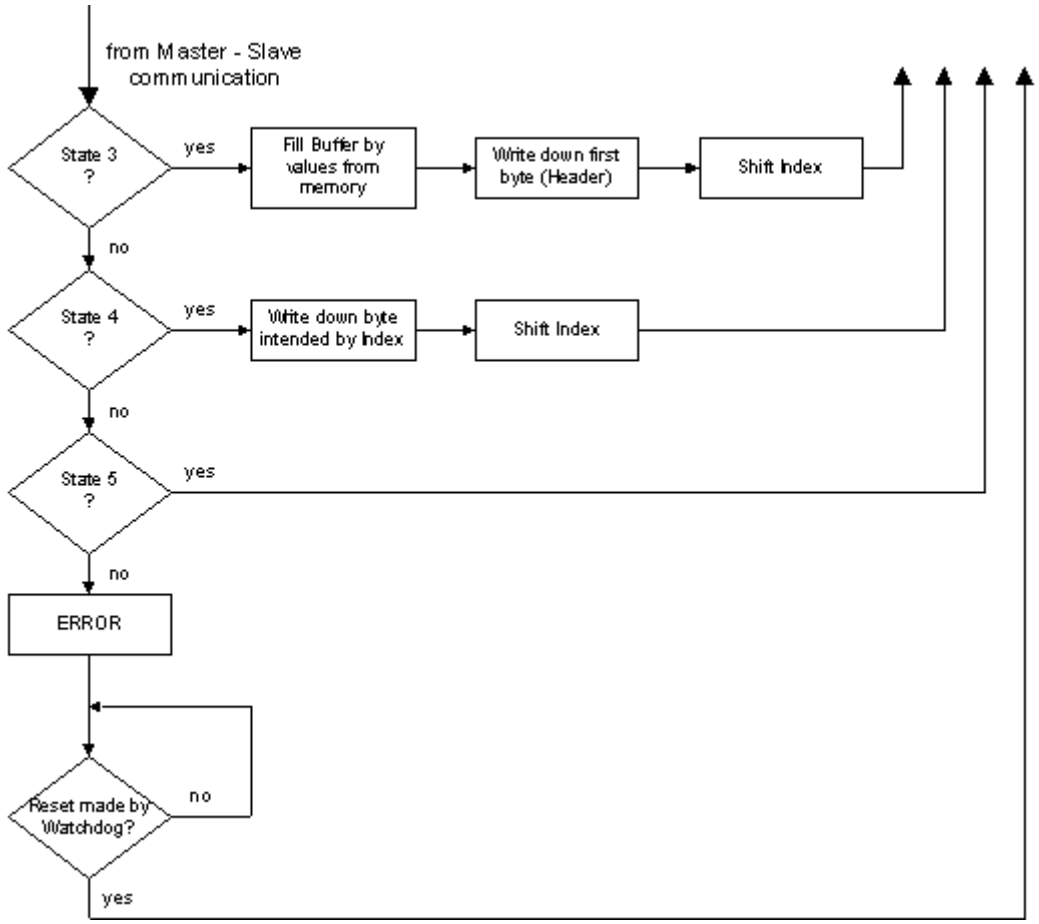


Fig 4.36 Communication from slave to master

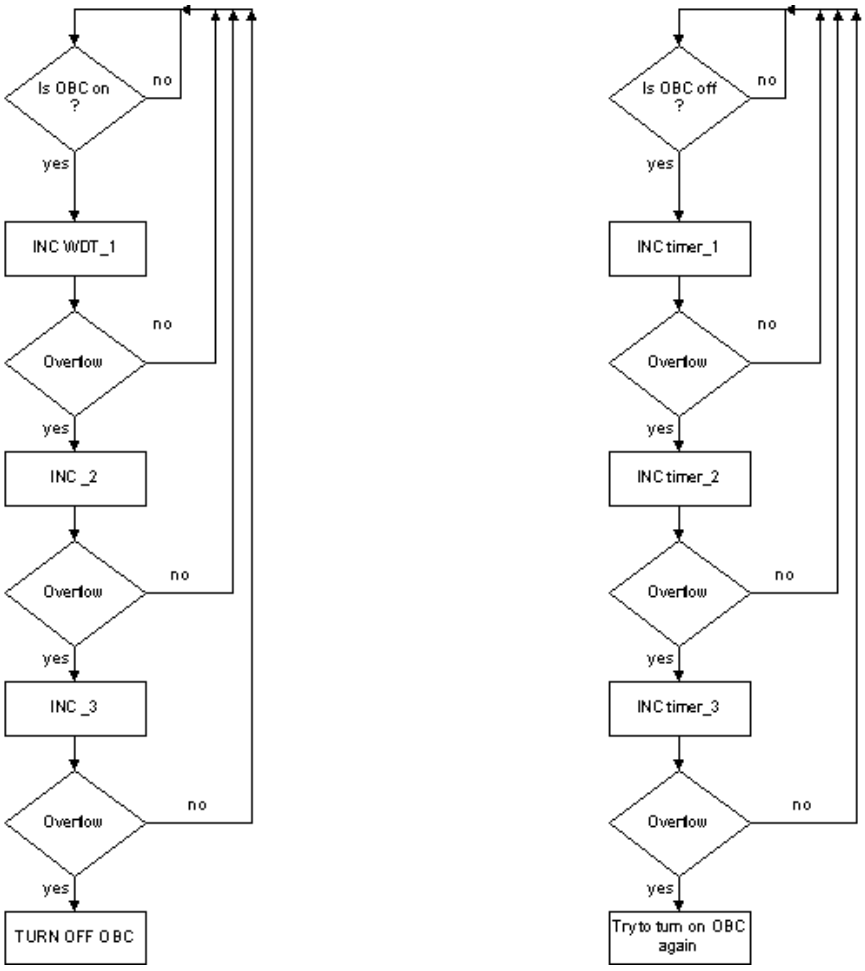
5. Special software for OBC

External watchdog and software timer

This program will provide watchdog for the OBC. As a reset of this watchdog serves any module received from the OBC. If the PSU will not receive anything from the OBC in 10 seconds, the program will turn-off OBC (put enable signal for OBC low state).

The OBC watchdog algorithm is depicted in figure 4.37a.

When OBC is turned off, the PSU itself must provide repeated turn-on signal after some time, which was decided to be 5 minutes. That is enough time to get out the OBC processor from dangerous states. The timer algorithm is described in figure 4.37b.



a b

Figure 4.37 OBC watchdog algorithm (a) OBC timer algorithm (b)

6. Arbitrage for MPPT signals

This part of software will guard signal from analog MPPT controller. If this signal is smaller than 30mV, program will turn-on software timer and after two minutes, if any signal is still not on analog MPPT, it will switch to another MPPT control source. If anytime in the future, an analog signal will be received from the MPPT, the program will switch back to it immediately.

7. Bootpin control

After the PSU receives module no. 30 from OBC (see table 4.9), the bootpin will be set to low level. When receiving module no. 31, the bootpin will be set to high level. The PSU will just follow the commands from OBC. After the reset of PSU's microcontroller, the bootpin will be set to low level.

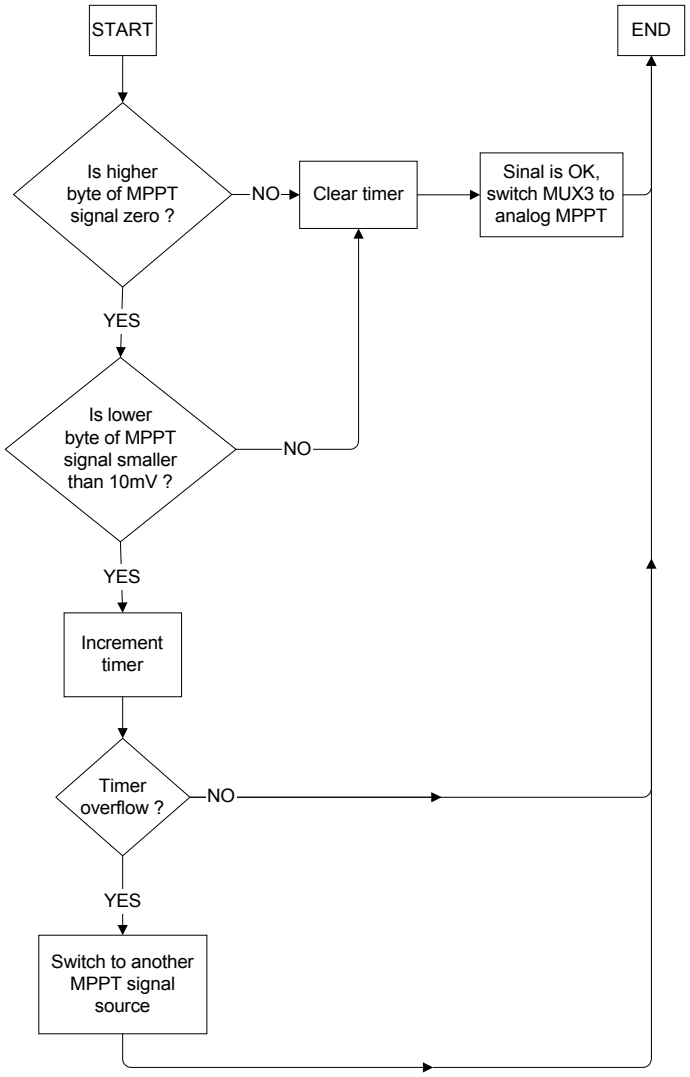


Figure 4.38 Testing algorithm for analog MPPT

8. Digital MPPT algorithm

The use of the microcontroller offers the possibility to implement a digital MPPT algorithm. Comparing to the analog one it has some significant advantages:

- Higher flexibility: it is very easy to add modifications and improvements for the algorithm.
- Lower size and mass: it is needed only the microcontroller and a operational amplifier with an input filter.

Everything is based on a fact that the used algorithm can be much more sophisticated than analog one. Of course, analog MPPT can be also very complex, but the weight and the size of system is increasing with complexity. In case of software it means few new rows in a program.

An *Incremental Conductance MPT Algorithm* (ICA) was chosen to implement. The biggest advantage of this new algorithm is, that when the proper value of maximum power point is found,

than there are no other losses. This algorithm consist in comparison new measured values with previous values.

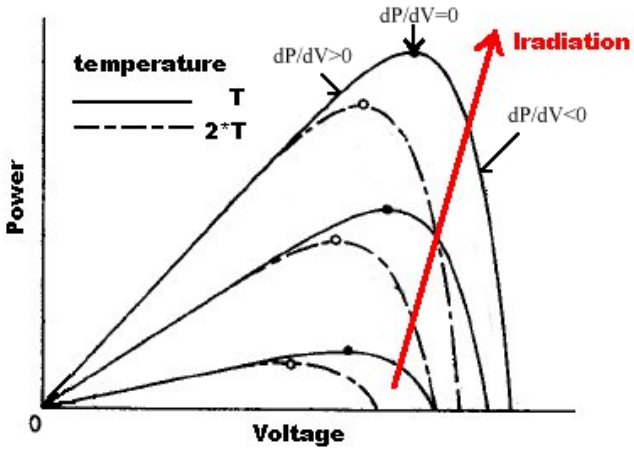


Figure 4.39 P-V curves for solar panels

As it can be seen on figure 4.39 *Maximum power operation point* (MPOP) is when $dP/dV = 0$. If the operation point is to the left of the MPOP then with increasing voltage the power is also increasing. If the operation point is to the right of the MPOP than the power is decreasing with increasing voltage. It can be written in this three formulas:

$dP/dV = 0$ at the MPOP,

$dP/dV > 0$ to the left of the MPOP,

$dP/dV < 0$ to the right of the MPOP.

If it is taken into account that $dP/dV = d(I \cdot V)/dV = I + V \cdot dI/dV$, than it is possible to rewrite previous equations as follow:

$dI/dV = -I/V$ at the MPOP,

$dI/dV > -I/V$ to the left of the MPOP,

$dI/dV < -I/V$ to the right of the MPOP.

In case of constant voltage, $dV = 0$, may change current its values. Than can be written relation for three possible conditions like this:

$dI = 0$ at the MPOP,

$dI > 0$ to the left of the MPOP,

$dI < 0$ to the right of the MPOP.

From all equations above can be easily drawn flowchart for ICA.

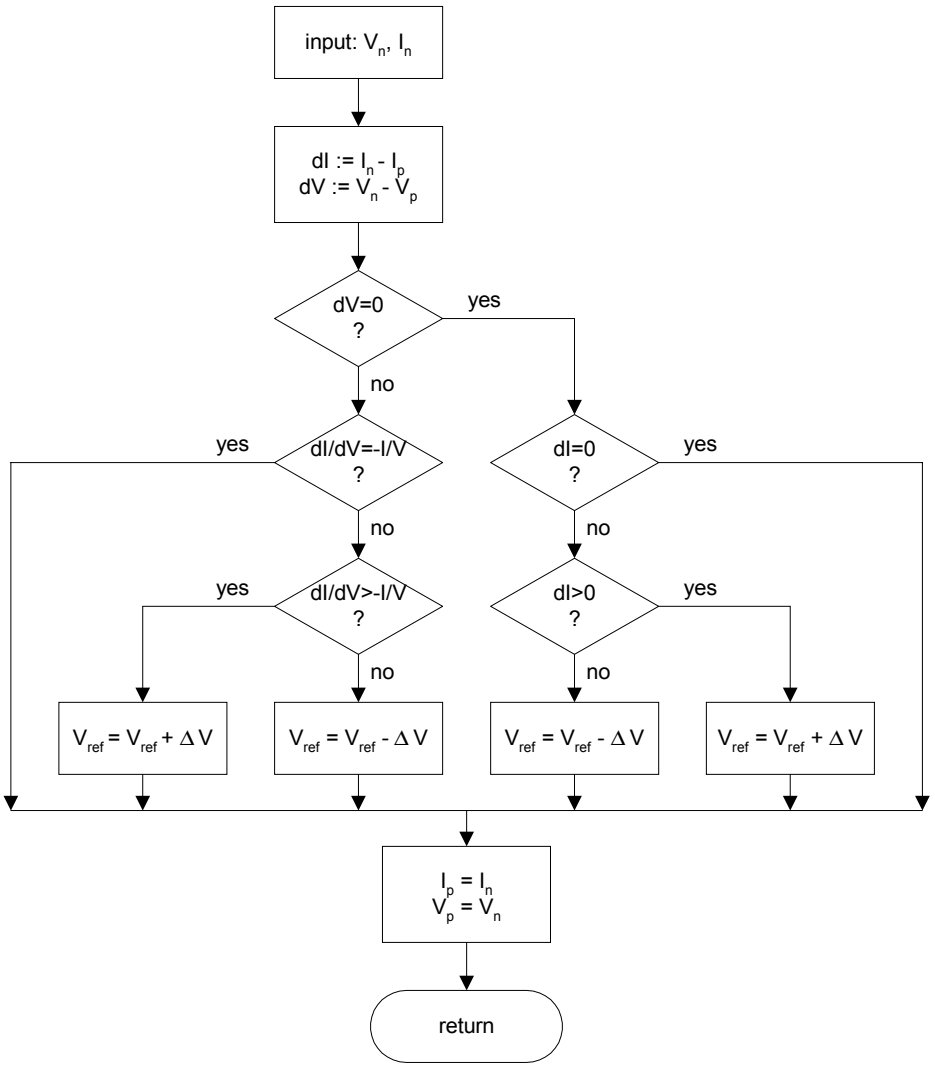


Figure 4.40 Flowchart for ICA

At the beginning of the algorithm is read the new values of I and V. Then is making differential of voltage and current by subtraction of new (n) and previous (p) values. Previous values are stored at the end of each preceding cycle. According to results from decision functions is set up a new value of reference voltage (V_{ref}) by either addition or deduction of nominal step $\Delta\mathbf{V}$.

4.9. Power supply for Power Supply Circuits

For supplying the circuits of the power supply it was chosen the linear regulator LM78L05 fed directly from the unregulated bus. Two main considerations were used for choosing this device. The first one was the small consumption of the circuits used in the interior of the power supply, so

the power loses due to the linear regulation are neglectable. The second one was the fact that this IC is self-protected in case of a shortcircuit at the output and overtemperature.

Linear regulator LM78L05

General Description

The LM78L05 is three terminal positive regulator. When used as a zener diode/resistor combination replacement, the LM78L05 usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. The regulator can provide local on card regulation, eliminating the distribution problems associated with single point regulation.

The LM78L05 is available in the plastic TO-92 (Z) package, the plastic SO-8 (M) package and a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. With adequate heat sinking the regulator can deliver 100mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- LM78L05 in micro SMD package
- Output voltage tolerances of ±5% over the temperature range
- Output current of 100mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and plastic SO-8 low profile packages
- No external components

Typical Application

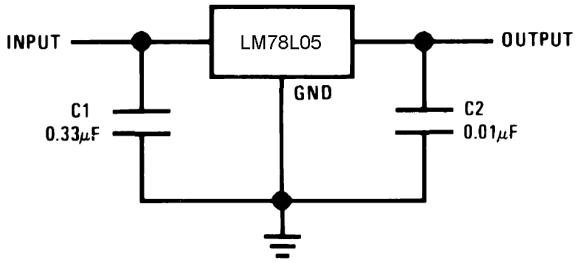


Figure 4.41 Typical application circuit for LM78L05

4.10. Summary

This chapter presents the implementation of the practical circuits that can be found in the power supply subsystem. All the most important modules have been detailed and computations performed. An important space is reserved for description of the devices used. It has been tried to use small outline components, due to the constrains about mass and geometrical dimensions for the power supply board, detailed previously in Chapter 2.

The functioning of the MCU used for the power supply board is described in section 4.9. Various flowcharts for specific parts of software are presented. Also, there is included an algorithm for the digital MPPT, as an alternative to the analog one, already implemented and described in section 4.1. For supplying the components on the board, it has been chosen a self-protected 5V integrated power supply, described briefly in section 4.9.